Analog Circuit Design in PD-SOI CMOS Technology for High Temperatures up to 400 °C using Reverse Body Biasing (RBB)

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Abstract

This work focuses on analog integrated CMOS (Complementary Metal-Oxide-Semiconductor) circuit design in SOI (Silicon on Insulator) technology for the use in high temperature applications. It investigates the influence of reverse body biasing (RBB) on the analog characteristics of SOI-MOSFET (Metal-Oxide-Semiconductor-Field-Effect-Transistor) transistors. Additionally, the enhancement of the operation capability of fundamental analog circuits at high temperatures up to 400 °C with the use of RBB is investigated.

Analog and digital integrated circuits are used in a variety of applications, e.g. consumer electronics or industrial measurement equipment. These integrated circuits have to work properly in the temperature range predefined by the application. As an example, operating temperatures reaching from −50 °C to 250 °C are required for geothermal drilling applications. Currently in the automotive industry, electronics have to operate reliably up to 150 °C and as control electronics are placed closer to the engine, a much higher operating temperature is required. High temperature electronics are also used in avionic- and space applications, e.g. for future venus exploration missions, where they have to withstand operating temperatures of 300 °C to 500 °C. Active or passive cooling of electronic components requires additional space and weight that increases the cost of the overall system. Cooling can be avoided in case electronics are capable of operating in harsh environmental conditions, i.e. at high temperatures.

SOI-MOSFET devices are theoretically capable of operation up to 400 °C or even higher, depending on the doping concentration of the silicon film. Nearly all material and device properties of importance to electronics worsen with increasing temperature, which is why 300 °C to 350 °C is the currently stated experimental maximum operating temperature of SOI devices. Analog circuit design up to the theoretical temperature limit exhibits severe limitations as SOI-MOSFET device characteristics are degenerated. SOI-MOSFET devices are partially depleted (PD) or fully depleted (FD), depending on the temperature, doping concentration of the silicon film, silicon film thickness and also channel length. FD devices offer a much

better analog performance compared to their partially depleted counterparts and are preferred for analog circuit design. In the considered SOI technology, SOI-MOSFET devices are FD at low temperatures and PD at high temperatures. The transition from FD to PD at high temperatures leads to increased device leakage currents and hence reduces the overall performance of the transistor devices. Thereby, the g_m/I_d factor as a major figure of merit is decreased dramatically at high temperatures. Especially the moderate inversion region, which offers high intrinsic gain and moderate intrinsic bandwidth, is strongly affected as device leakage currents exceed the range of device operating currents at high temperatures.

Reverse body biasing (RBB) refers to the reverse biasing of the film-source PN-junction of a MOSFET transistor. In recent works, reverse body biasing has been applied to digital circuits in order to reduce the static current consumption. Reverse body biasing has also been investigated in the analog domain. Nevertheless, the importance of the technique to realize analog circuits capable of operating at the theoretical temperature limit of SOI technology has not been identified yet. SOI-MOSFET devices with an H-shaped gate are investigated in a 1.0 µm PD-SOI technology. These devices provide a body-contact, which is used to apply the reverse body bias. It is found that due to the use of RBB, these devices remain fully depleted in the considered temperature range up to 400 °C. Due to the reduction of leakage currents, reverse biased SOI-MOSFET devices are capable of operating in the mid moderate inversion region, with an operating current of one fifth of the leakage current level which was measured without RBB. This results in an improved g_m/I_d factor and an increase of the intrinsic gain by approximately 14 dB. Besides the investigation of SOI-MOSFET device characteristics, reverse body biasing is also applied to fundamental analog building blocks, e.g. an analog switch, current mirrors, a two-stage operational amplifier and a first order bandgap voltage reference. It is found that reverse body biasing significantly improves the high temperature operation of these circuits. In summary, the proposed technique of reverse body biasing offers the possibility to achieve FD device characteristics in a PD-SOI technology and thereby to improve the performance of analog circuits at high temperatures up to 400 °C.

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Abbrevations

ABB	Adaptive body biasing
AC	Alternating current
ADC	Analog-to-digital converter
B	Body terminal
BEX	Mobility temperature exponent
BG	Back gate terminal
BJT	Bipolar junction transistor
BNC	Bayonet Neill Concelman connector
BPSG	Borophosphosilicate glass
BSIMSOI	BSIMSOI is a SPICE compact model for SOI circuit design
BT PD-SOI ...	Body tied partially depleted silicon on insulator
CLM	Channel length modulation
CM	Current mirror
CMOS	Complementary metal-oxide-semiconductor
D	Drain terminal
DC	Direct current
DD	Dynamically depleted
DIBL	Drain-induced barrier lowering

EEPROM ..... Electronically erasable and programmable read only memory

FBB ..... Forward body biasing

FD ..... Fully depleted

FinFET ..... Fin field-effect-transistor

FOX ..... Field-oxide

G ..... Gate terminal

GOX ..... Gate oxide

GPIB ..... General purpose interface bus / IEEE-488

HGATE ..... H-shaped gate SOI-MOSFET

HT ..... High temperature

IC ..... Inversion coefficient

`Isbjt` ..... BSIMSOI model parameter for BJT injection saturation current

`Isrec` ..... BSIMSOI model parameter for recombination in depletion saturation

`K1` ..... BSIMSOI model parameter for first order body effect coefficient

LOCOS ..... Local oxidation of silicon

MI ..... Moderate inversion

MOSFET ..... Metal-oxide-semiconductor-field-effect-transistor

`Nch` ..... BSIMSOI model parameter for the doping concentration of the silicon film

`Nfactor` ..... BSIMSOI model parameter for the subthreshold swing factor

NHGATE ..... N-channel HGATE SOI-MOSFET

NSOI	N-channel Split-Source SOI-MOSFET
op-amp	Operational amplifier
PCB	Printed circuit board
PD	Partially depleted
PHGATE	P-channel HGATE SOI-MOSFET
PID-Controller	Proportional-integral-derivative controller
PSOI	P-channel Split-Source SOI-MOSFET
PTAT	Proportional to absolute temperate
PoR	Power-on reset
RBB	Reverse body biasing
RF	Radio frequency
RFID	Radio frequency identification
RPOLY	Poly-silicon resistor
RPPLUS	P^+ implanted resistor
S	Source terminal
SCE	Short-channel-effects
SI	Strong inversion
SIMOX	Separation by implantation of oxygen
SOI	Silicon on insulator
`soimod`	BSIMSOI model selector
SSCB	Silicon sidewall body contact
`Tbox`	BSIMSOI model parameter for the buried oxide thickness
`Tox`	BSIMSOI model parameter for the gate oxide thickness

`Tsi`	BSIMSOI model parameter for the silicon film thickness
UTB	Ultra thin body
VLSI	Very large scale integration
WI	Weak inversion
ZTC	Zero temperature coefficient

List of Symbols

β	Bipolar current gain
χ_{SI}	Electron affinity of silicon
$\Delta\phi$	Portion of surface potential to reach strong inversion
ΔV_{bi}	Built-in potential lowering in FD SOI-MOSFETs
ϵ_0	Dielectric constant in vacuum $8.85 \cdot 10^{-9}\ \frac{\mathrm{F}}{\mathrm{m}}$
ϵ_{ox}	Dielectric constant of silicon-oxide $3.9 \cdot \epsilon_0$
ϵ_{si}	Dielectric constant of silicon $11.9 \cdot \epsilon_0$
γ	Body effect coefficient
$\hat{C}_{GBi}$	Intrinsic gate-body capacitance normalized to the gate-oxide capacitance
$\hat{C}_{GSi}$	Intrinsic gate-source capacitance normalized to the gate-oxide capacitance
λ	Channel length modulation factor
μ_0	Zero-field mobility of charge carriers
μ_{T0}	Zero-field mobility of charge carriers at 300K
$\phi(x)$	Surface potential as a function of silicon film depth
ϕ_F	Fermi potential
ϕ_S	Surface potential
ϕ_{bi}	Built-in potential of a pn-junction
ϕ_{Fn}	Fermi potential of a n-type semiconductor
ϕ_{Fp}	Fermi potential of a p-type semiconductor
ϕ_{ms1}	Front gate metal semiconductor work function difference
ϕ_{ms2}	Back gate metal semiconductor work function difference

ϕ_{ms} ..... Metal semiconductor work function difference

ϕ_{S1} ..... Front gate surface potential

ϕ_{S2} ..... Back gate surface potential

τ_g ..... Lifetime of generated charges in the depletion region

τ_n ..... Lifetime of electrons

τ_p ..... Lifetime of holes

A_i ..... Intrinsic gain

C'_D ..... Depletion capacitance per unit area

C'_{OX1} ..... Front gate oxide capacitance per unit area

C'_{OX2} ..... Back gate oxide capacitance per unit area

C_{DBi} ..... Intrinsic drain-body capacitance

C_{DSi} ..... Intrinsic drain-source capacitance

C_{GBi} ..... Intrinsic gate-body capacitance

C_{GDi} ..... Intrinsic gate-drain capacitance

C_{GSi} ..... Intrinsic gate-source capacitance

C_L ..... Load capacitance

C_{OX1} ..... Front gate oxide capacitance

C_{OX2} ..... Back gate oxide capacitance

C_{SBi} ..... Intrinsic source-body capacitance

C_{si} ..... Capacitance of the fully depleted silicon film

D_n ..... Diffusion constant of electrons

E ..... Energy level

E_C ..... Conduction band energy

$E_G(0)$ ..... Bandgap energy at absolute zero temperature (0 K)

E_V ..... Valence band energy

E_F ..... Fermi energy

E_G ..... Bandgap energy

E_i ..... Intrinsic Fermi energy level

F_E ..... Fermi-Dirac distribution function

f_T ..... Intrinsic bandwidth / Transition frequency

g_m/I_d ..... Transconductance efficiency

g_{ds} ..... Drain-source small signal conductance

g_{mb} ..... Body-source small signal transconductance

g_{mMAX} ..... Maximum small signal transconductance

g_m ..... Small signal transconductance

I_0 ..... Technology current

I_0 (fit) ..... Technology current used for fitting

i_f ..... Specific current, equivalent to I_0

I_{Bbjt} ..... Base current of parasitic bipolar transistor

I_B ..... Body current

I_{CH} ..... Current in the inverted channel

I_C ..... Collector current

I_{DIFF} ..... Diffusion current

I_{dsat} ..... Saturation current

I_d ..... Drain current

I_E ..... Emitter current

I_{Gmax} ..... Generation current at maximum depletion depth

I_G ..... Generation current

I_{ii} ..... Impact ionization current

I_{IN} ..... Input current

I_L ..... Leakage current

I_{OFF} ..... MOSFET off-state current

I_{ON} ..... MOSFET on-state current

I_{OUT} ..... Output current

I_{PN-N} ..... PN-junction leakage current of N-channel device

I_{PN-P} ..... PN-junction leakage current of P-channel device

I_{PN} ..... PN-junction leakage current

I_{PTAT} ..... Proportional to absolute temperature current

I_{Sub-N} ..... Subthreshold leakage current of N-channel device

I_{Sub-P} ..... Subthreshold leakage current of P-channel device

I_{Sub} ..... Subthreshold leakage current

I_S ..... Source current

k ..... Boltzmann constant $8.617 \cdot 10^{-5} \frac{\mathrm{eV}}{\mathrm{K}}$

L ..... Channel length

L_B ..... Base region length

L_n ..... Diffusion length of electrons

n ..... Body factor

$n\,(\mathrm{fit})$ ..... Body factor used for fitting

N_A ..... Doping concentration of p-type silicon

N_{CH} ..... Channel doping concentration

N_{DRAIN} ..... Doping concentration of drain region

N_D ..... Doping concentration of n-type silicon

n_{FD} ..... Body factor in fully depleted mode

N_I ..... Intrinsic region in PIN-diodes

n_i ..... Intrinsic carrier concentration

n_{n0} ..... Electron concentration in n-type silicon

n_{p0} ..... Electron concentration in p-type silicon

n_{PD} ..... Body factor in partially depleted mode

N_{SOURCE} ... Doping concentration of source region

N_{Sub} ..... Effective substrate doping concentration

p_{n0} ..... Hole concentration in n-type silicon

p_{p0} ..... Hole concentration in p-type silicon

q ..... Electron charge $1.602 \cdot 10^{-19}\,\mathrm{C}$

Q'_d ..... Depletion charge per unit area

Q_d ..... Depletion charge

Q_{ox1} ..... Front gate oxide charges

Q_{ox2} ..... Back gate oxide charges

R_B ..... Body resistance

r_{ds} ..... Small signal drain-source resistance

R_L ..... Load resistance

R_{out} ..... Output resistance

R_S ..... Source resistance

S ..... Subthreshold swing

S_{FD} ..... Subthreshold swing in fully depleted mode

S_{PD} ..... Subthreshold swing in partially depleted mode

T ..... Temperature

T_0 ..... Reference temperature

T_t ..... Transition temperature

t_{BOX} ..... Back gate oxide (buried oxide) thickness

t_{OX1} ..... Front gate oxide thickness

t_{SI} ..... Silicon film thickness

TK_1 ..... First order (linear) temperature coefficient

TK_2 ..... Second order (quadratic) temperature coefficient

V_A ..... Early voltage

V_b ..... Body potential

V_t ..... Thermal voltage

V_{BGS} ..... Back gate-source voltage

V_{bi} ..... Built-in voltage of a pn-junction

V_{BN} ..... Body bias voltage for N-channel devices

V_{BP} ..... Body bias voltage for P-channel devices

V_{BSminN} .... Required minimum reverse bias voltage for N-channel devices

V_{BSminP} ..... Required minimum reverse bias voltage for P-channel devices

V_{BSmin} ..... Required minimum reverse bias voltage

V_{BSN} ..... Body-source voltage for N-channel devices

V_{BSP} ..... Body-source voltage for P-channel devices

V_{BS} ..... External body-source voltage

v_{bs} ..... Small signal body-source voltage

V_{CM} ..... Common mode voltage

V_{DDA} ..... Supply voltage of analog circuits

V_{DSsat} ..... Drain-source saturation voltage

V_{DS} ..... Drain-source voltage

v_{ds} ..... Small signal drain-source voltage

V_{FB1} ..... Front gate flatband voltage

V_{FB2} ..... Back gate flatband voltage

V_{FB} ..... Flatband voltage

V_{G1} ..... Front gate voltage

V_{G2acc} ..... Back gate voltage, at which the back interface becomes accumulated

V_{G2} ..... Back gate voltage

V_{GNDA} ..... Ground potential in analog circuits

V_{GS1} ..... Front gate-source voltage

V_{GS} ..... Gate-source voltage

v_{gs} ..... Small signal gate-source voltage

V_{IN} ..... Input voltage

v_{in} ..... Small signal input voltage

V_{OUT} ..... Output voltage

v_{out} ..... Small signal output voltage

V_{REF} ..... Reference output voltage

V_{th1} ..... Front gate threshold voltage

V_{th2} ..... Back gate threshold voltage

W ..... Channel width

W_{eff} ..... Effective channel width

x_{d1max} ..... Front gate depletion depth in strong inversion

x_{d1} ..... Front gate depletion depth

x_{d2} ..... Back gate depletion depth

phi ..... clock signal for analog switch

sgn ..... Signum function

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Chapter 1

Introduction

1.1 Motivation

Analog and digital integrated circuits are used in a variety of applications, e.g. consumer electronics or industrial measurement equipment. These integrated circuits have to work reliably in the temperature range specified by the application. Figure 1.1 shows the different temperature ranges of electronics, according to their application. Currently in the automotive industry, electronics have to operate up to a temperature of 150 °C [Aut03] [JEJ+04].

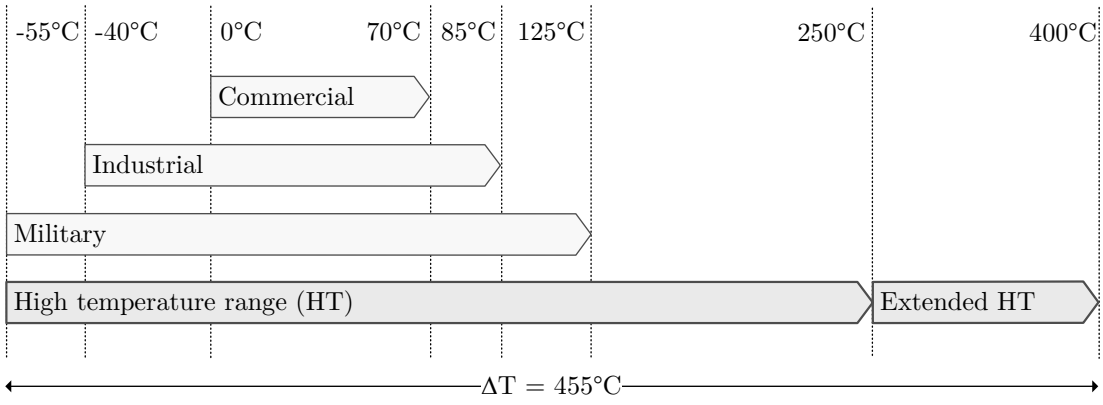

Figure 1.1: Operating temperature ranges according to their specific application.

As the automotive industry is migrating from mechanical or hydraulic to electromechanical systems, it is required to place sensors systems, control electronics and signal conditioning electronics closer to the heat sources inside the vehicle [WC12]. Active or passive cooling of the electronic components requires additional space and weight and it thereby increases the costs of the overall

system. Cooling can be avoided in case electronics are capable of operating in harsh environmental conditions, i.e. at high temperatures. In some application, active cooling is not possible and passive cooling is not effective, e.g. in geothermal drilling applications [WC12]. These applications require temperature ranges reaching from −50 °C to 250 °C, while the temperature range is currently being extended up to 300 °C [Est13] [Mac13].

High temperature electronics are also used in avionic systems and are necessary for space exploration missions planed by the National Aeronautics and Space Administration (NASA), i.e. for the Venus In Situ Exploration (VISE), Venus Mobile Explorer (VME) and the Venus Surface Sample Return (VSSR) missions [Kol07]. Operating temperatures of 300 °C to 500 °C are required for these missions. As avionic- and spacecraft systems need to be lightweight in order to reduce costs, active or passive cooling of electronic components remains cost-intensive. Within avionic systems, the complexity of interconnections can be significantly reduced by placing engine control systems closer to the engine, i.e. inside the high temperature environment [MB06]. With reduced interconnects, the weight is reduced, while the system reliability is increased [MB06] [WC12]. In summary, there is an increasing industry demand for high temperature electronics operating above 300 °C. This trend is also shown in Figure 1.2. The overall demand is small but increasing continuously.

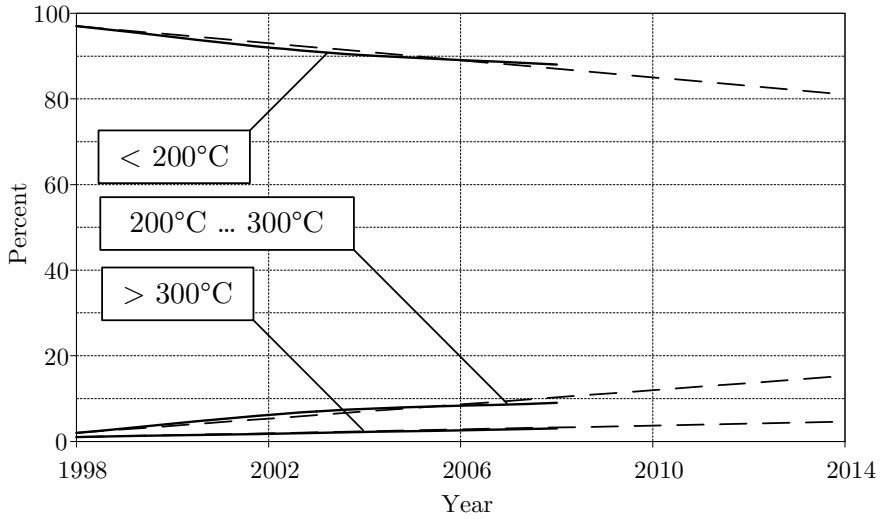

Figure 1.2: Demand for high temperature electronics divided into operating temperature ranges [Wil02].

Harsh environmental conditions, e.g. high temperature or high pressure, affect the reliability of integrated circuits and even lead to failure of operation. In order to meet the specifications for high temperature applications, the use of

integrated circuits manufactured in SOI CMOS (Silicon on Insulator Complementary Metal-Oxide-Semiconductor) technology is preferred over standard bulk CMOS technology. Due to reduced leakage currents and higher operating speeds with the same amount of required power, SOI technology is well suited for high temperature conditions [Col04]. SOI-MOSFET (Metal-Oxide-Semiconductor-Field-Effect-Transistor) devices are theoretically capable of operation up to 400 °C or even higher, depending on the doping concentration of the silicon film. However, 300 °C to 350 °C is the currently stated experimental maximum operating temperature [Kol07] [FNH05]. Nearly all material and device properties of importance to electronics worsen with increasing temperature [Kir98]. As a result, analog circuit design up to the theoretical temperature limit of 400 °C exhibits severe limitations as SOI-MOSFET device characteristics are degenerated.

At high temperature operation, high leakage currents within integrated circuits lead to reduced accuracy and also cause malfunctions. Therefore, leakage currents have to be considered as a major source of error in high temperature analog circuits. The degradation of intrinsic gain and bandwidth of SOI-MOSFET devices at high temperatures also have to be considered when designing analog circuits for high temperatures. Since technology improvements are only capable of reducing leakage currents by a limited amount, advanced design techniques are required to eliminate the resulting effects. Solving these issues will allow analog circuit design in SOI technology up to its theoretical temperature limit. This implies the reduction of leakage currents within the prospects of circuit design in the first place, followed by the compensation of remaining leakages with compensation structures that are brought into the circuit. Furthermore, a new approach to improve the intrinsic gain and bandwidth of the transistor devices at high temperatures is also required.

SOI-MOSFET devices are partially depleted (PD) or fully depleted (FD), depending on the temperature, doping concentration of the silicon film, silicon film thickness and also the channel length [APPC04] [FNH05]. It is well known that fully depleted devices offer a much better analog performance, e.g. higher subthreshold slope, compared to their partially depleted counterparts and are therefore preferred for analog circuit design [FNH05] [Col04] [KS98].

In the considered Fraunhofer IMS 1.0 µm SOI technology, with a film thickness of 150 nm, SOI-MOSFET devices are fully depleted at low temperatures and partially depleted at high temperatures. Device leakage currents are increased and the overall performance of SOI-MOSFET devices is reduced due to the transition from fully depleted to partially depleted at high temperatures. Thereby, the g_m/I_d

factor as a major figure of merit is decreased dramatically at high temperatures [EVJR09]. Especially the moderate inversion region, which offers high intrinsic gain and moderate intrinsic bandwidth, is strongly affected as device leakage currents exceed the range of device operating currents at high temperatures. Due to leakage currents, the moderate inversion region cannot be used at high temperatures, although it is the desired point of operation [Bin07b]. Especially for applications where gain errors need to be minimized, the required gain cannot be achieved due to the degradation of the g_m/I_d factor.

As a consequence, high drain currents are required to keep a sufficient safety margin to the leakage current level. This also affects the overall power consumption of analog circuits working at high temperatures. Increased leakage currents of SOI-MOSFETs result in poor I_{ON}/I_{OFF} ratios and lead to an increased static current consumption of analog and digital circuits [FNH05]. Since the threshold voltage of partially depleted devices decreases non-linearly with increasing temperature, SOI-MOSFET devices become self-conducting at high temperatures. High threshold voltages are therefore required to keep subthreshold leakage currents small and to be able to operate the devices up to very high temperatures [FNH05]. Decreasing the overall supply voltage for decreased power consumption can therefore not easily be realized.

Reverse body biasing (RBB) refers to the reverse biasing of the film-source PN-junction of a MOSFET transistor. In recent works, reverse body biasing has been applied to digital circuits in order to reduce the static current consumption. It has also been applied to improve the threshold voltage of SOI-MOSFET devices in analog circuits. However, the importance of this technique to realize analog circuits, which are capable of operating at the theoretical temperature limit of SOI technology has not been identified yet.

1.2 State of the Art

The DC and RF behavior of SOI-MOSFET devices at high temperatures has been studied intensively in recent works [ECF+96] [EHT+05] [GKH+08] [EVJR09] [VJEKSM08]. The floating body effect, which is responsible for the degradation of the device's analog performance has also been reported for fully depleted SOI-MOSFET devices [HCA+94][PNWP94] [CSW+04]. Nevertheless, FD devices offer much better analog performance compared to PD devices.

Current research activities in the field of SOI semiconductor devices for VLSI (Very Large Scale Integration) integrated circuits are concerning ultra thin body

(UTB) devices with a film thickness of several nanometers. Investigations of planar FD-SOI high temperature devices with film thickness in the range of 6 nm . . . 7 nm have also been reported [SIM+13] [KAFF11]. 3D FinFET devices in bulk silicon technology and SOI technology are currently available, and operate within the temperature range of commercial electronics. Ongoing research aims to further decrease device sizes towards future technology nodes [War13]. The high temperature behavior of FinFET devices has also been investigated up to 300 °C [TPM+08] [AMS+07] [MWC+06]. However, state of the art high temperature and high voltage integrated circuits are using the 1.0 µm SOI technology node while downsizing to 350 nm is currently in progress [LNC+03]. High temperature SOI processes currently offer operation of integrated circuits up to a temperature of 250 °C while operation up to 300 °C is pursued. The currently stated experimental temperature limit of PD-SOI technology is estimated to lie in the range of 300 °C to 350 °C, depending on the doping concentration of the silicon film [NOC02] [Col04] [FNH05] [Com95]. In a fully depleted thin film SOI technology, an experimental maximum operating temperature range of 400 °C has been reported [Col98]. Nevertheless, depending on the doping concentration of the silicon film, these fully depleted processes require film thicknesses of 50 nm or below [FNH05].

SOI technology cannot easily be used beyond temperatures of around 400 °C to 425 °C, as the silicon base material becomes intrinsic. Wide bandgap materials, e.g. Gallium-Nitride (GaN) oder Silicon-Carbide (SiC) offer higher operating temperatures compared to SOI technology [NOC02]. Silicon-Carbide promises an upper operating temperature of approximately 600 °C [WFWS06]. With the use of diamond substrates, an estimated theoretical operating temperature of 1000 °C seems feasible [WFWS06]. Nevertheless, wide bandgap integrated circuits with the complexity of todays SOI circuits are far from realization. Also the fabrication costs of integrated circuits manufactured in wide-bandgap technologies are much high compared to SOI technology.

Body biasing (BB) has been found useful in influencing the threshold voltage, the frequency characteristics and the breakdown voltage of SOI-MOSFET devices [MHY+99] [GMT11]. A distinction can be made between forward body biasing (FBB) and reverse body biasing (RBB). Reverse body biasing is well known for reducing the off-state leakage current in digital circuits [ABS+05] [NR03] [GKH+08] [LNL+02], whereas FBB can be used to improve the driving capability of SOI-MOSFET devices. Additionally, it has also been shown how the ZTC (Zero Temperature Coefficient) point of an SOI-MOSFET device can be influenced using body biasing in order to realize ZTC voltage references for high temperatures

[EKDSM+08]. Different body contact geometries and models have been recently investigated to improve the effectiveness of body biasing [DAK10] [SFAH99].

Analog circuit components as well as digital circuit components are required to realize complex integrated circuits. Analog components are also required to support the operation of digital circuits, as they rely on clock generators, power-on reset (PoR) circuits, voltage regulators, etc. In 1995, the improvement of analog circuit performance at high temperatures has been declared as one of the most important long-term research needs for high temperature electronics [Com95]. Essential circuit requirements include on-chip voltage references, wideband operational amplifiers, low-leakage switches and sample-and-hold circuits, which all are required for high resolution analog-to-digital converters (ADC) [Com95].

These analog-to-digital converters are required in order to provide digital sensor output data in sensor systems. Current state of the art high temperature analog-to-digital converters are featuring accuracies of 13 bit [DF03] and 12 bit [Rom09] in sigma-delta and successive approximation topologies, respectively. The maximum operating temperature of these analog-to-digital converters is 255 °C [Rom09]. Operational amplifiers are necessary in many different analog applications and are also used in analog-to-digital converters. Commercially available operational amplifiers state a maximum operating temperature of 225 °C [OLE05] but have also been tested up to 300 °C [Ohm12].

Voltage references are essential analog building blocks as they provide reference voltages required for a variety of applications. Reference voltages need to be stable over a wide temperature range. The rejection of supply voltage and temperature variations are the primary figure of merit for these voltage references. A precise bandgap voltage reference with an accuracy of < 1 ppm/K, capable to operate up to 130 °C has been reported by Liu et al. [LLLZ10]. Bandgap voltage references with an accuracy of 40 ppm/K for a maximum temperature of 250 °C [Ohm06] and a temperature coefficient of 138 ppm/K up to 300 °C [PXL+12] were also reported recently. To our best knowledge, a PD-SOI voltage reference, capable of operation up to up to 400 °C, has not yet been presented. Operation near the theoretical temperature limit of SOI technology is so far restricted to fully depleted SOI-MOSFET devices only. However, FD-SOI technologies have to provide an ultra thin body (UTB), which is cost intensive and results in strong threshold voltage variations as relative film-thickness mismatches increase. In the presented work, the use of RBB in a partially depleted SOI technology with a film thickness of 150 nm is investigated at high temperatures in order to overcome the requirement of an ultra thin silicon film. The focus thereby is on the theoretical

investigation on the impact of RBB on SOI-MOSFET device characteristics at high temperatures. All theoretical results are proven by experimental results. A circuit design approach, to implement RBB in fundamental analog circuits is also presented in this work.

1.3 Thesis Outline

This work is structured as follows: Chapter 2 describes the considered SOI technology. Geometries and doping concentration of all SOI devices within the technology are given as needed for various calculations throughout this work. Chapter 3 focuses on fundamental SOI-MOSFET device physics and effects in order to prepare the discussion in the following chapters. In Chapter 4, these basic device characteristics are reviewed with respect to the operation at high temperatures. Temperature dependencies and the degradation of essential analog parameters at high temperatures are presented in detail. The resulting consequences for analog circuits utilizing SOI-MOSFET devices are demonstrated in Chapter 5. How the SOI-MOSFET device characteristics at high temperatures are improved by reverse body biasing is explained in detail in Chapter 6. A first approach to implement RBB in fundamental analog circuits is presented in Chapter 7. The improved operation capability of analog circuits with applied RBB is then also demonstrated experimentally in Chapter 7. Chapter 8 finally summarizes all results and presents a proposal on future work in this research field.

Chapter 2

SOI CMOS Technology

The high temperature characteristics of transistor devices fabricated in a bulk silicon CMOS technology have been studied intensively up to 300 °C by F. S. Shoucair in 1984 [SE84][SWP84b][SWP84c]. Leakage current mechanisms, the effect on small signal parameters of MOSFETs, as well as considerations for analog circuit design at high temperatures have then been developed later on by F. S. Shoucair and J.M. Early from 1984 to 1989 [SWP84a] [Sho86] [Sho89]. In an SOI technology, separation of each transistor device is supported by an insulating layer beneath a conducting silicon film and laterally by the field-oxide extending down to the buried oxide. Thereby, transistors manufactured in an SOI technology are electrically and thermally isolated [Col04]. Compared to a bulk silicon technology, parasitic effects like *latchup* can be effectively eliminated due to the isolation of SOI-MOSFET devices [Col04]. Figure 2.1 show a cross section of N-channel MOSFETs in bulk silicon technology (a) and SOI technology (b), respectively.

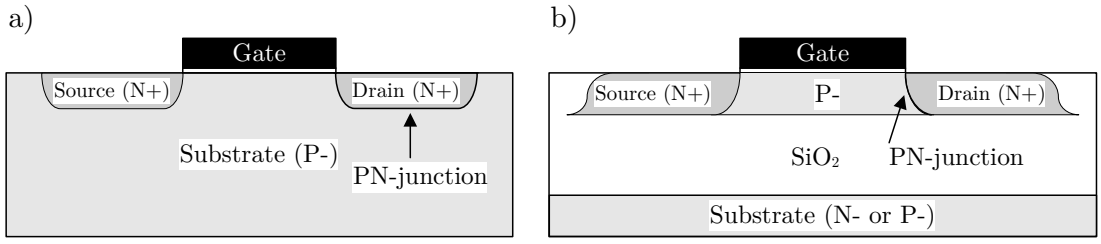

Figure 2.1: MOSFET structure a) in bulk silicon CMOS technology and b) in SOI CMOS technology.

It can be seen in Figure 2.1 that the insulating layer in SOI technology reduces the effective PN-junction area at the drain and source side of the transistor. Thereby, the effective reverse currents of the drain- and source diodes are reduced significantly in SOI technology [IRS+03] [Col04]. Also the parasitic capacitance of

the source and drain regions to the substrate can be reduced by a factor of 4 to 7 using SOI technology [Col04]. Due to the reduction of parasitic capacitance, SOI circuits show improved circuit speeds compared to their bulk silicon counterparts [Col04]. The superiority of SOI over bulk silicon technology at high temperatures is very well known and is not further discussed in this work [FECJ94] [SGGW04] [EVJR09] [KNV+03].

2.1 Devices in SOI CMOS Technology

Different types of semiconductor devices in the considered SOI technology are presented in this section, including dimensions and doping concentrations in order to prepare the discussion of SOI-MOSFET fundamental device physics in the following chapters. *Smart Cut*[1] processed SOI wafers are used as a base material for the fabrication process. The SOI technology considered for the investigations in this work is the Fraunhofer IMS 1.0 µm PD-SOI CMOS technology. It features 3 layers of tungsten metalization, namely M1, M2 and M3. A cross section of the entire process stack is shown in Figure 2.2.

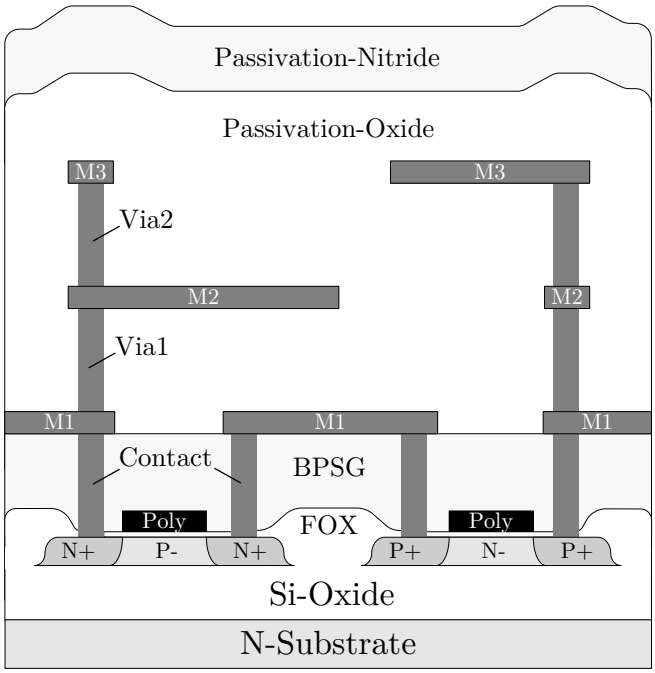

Figure 2.2: Cross section of the 1.0 µm PD-SOI technology.

[1] *Smart Cut* is a registered trademark of S.O.I.TEC SILICON ON INSULATOR TECHNOLOGIES (SOITEC, SA).

The metalization layers are interconnected by vias, namely Via1 and Via2. A contact layer connects M1 with the active source and drain regions, as well as with the poly-silicon gate of the device. In Figure 2.2, FOX is the field-oxide and BPSG is the borophosphosilicate glass. The technology also features high voltage SOI-MOSFET devices, poly/N^+ capacitors, single poly EEPROM cells, Zener-diodes and PIN-diodes. A cross section of an SOI-MOSFET with Gate (G), Source (S), Drain (D) and Back-gate (BG) terminals is shown in Figure 2.3.

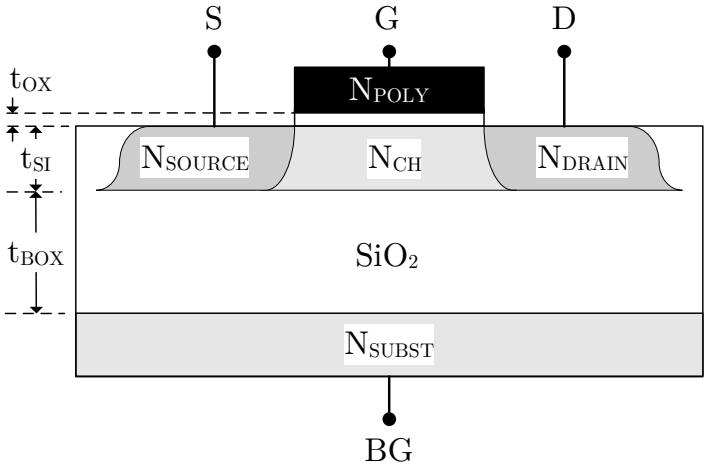

Figure 2.3: Cross section of an SOI-MOSFET device, corresponding layer thicknesses and doping concentrations.

The silicon film thickness t_{SI} is 150 nm, the front gate oxide t_{OX} is 40 nm and the buried oxide thickness t_{BOX} is 400 nm.

For N-channel SOI-MOSFETs, the channel doping type N_{CH} is P^-, whereby source- and drain doping types N_{SOURCE} and N_{DRAIN} are N^+. The qualitative non-uniformly channel doping concentrations N_{CH} as a function of silicon film depth of N-channel and P-channel SOI-MOSFETs are shown in Figure 2.4.

An effective uniformly distributed doping concentration of $N_{CH} = N_D \approx 1.8 \cdot 10^{16}\,\mathrm{cm}^{-3}$ is determined for analytical considerations of the P-channel SOI-MOSFET device physics. For the N-channel SOI-MOSFET an effective uniformly distributed doping concentration of $N_{CH} = N_A \approx 3 \cdot 10^{16}\,\mathrm{cm}^{-3}$ is assumed.

2.1.1 Split-Source Transistor

Figure 2.5 illustrates the top view of the Split-Source N-channel SOI-MOSFET, from now on referred to as NSOI. The silicon film (body) of the transistor is contacted by highly implanted P^+ body-contacts on the source side of the transistor. Source and body are then short-circuited by the source contact. Due

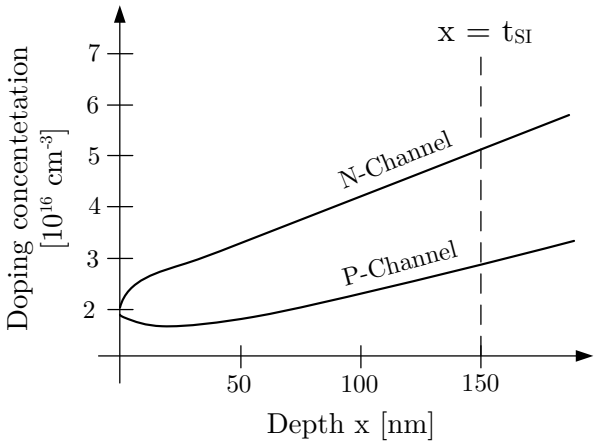

Figure 2.4: Qualitative doping concentration of P-channel ($N_{CH} = N_D$) and N-channel SOI-MOSFETs ($N_{CH} = N_A$) over silicon film depth x.

to the body contact, the effective width W_{eff} of the N^+ implanted source is smaller than the width of the N^+ implanted drain. If the transistor width is increased, additional body contacts are inserted.

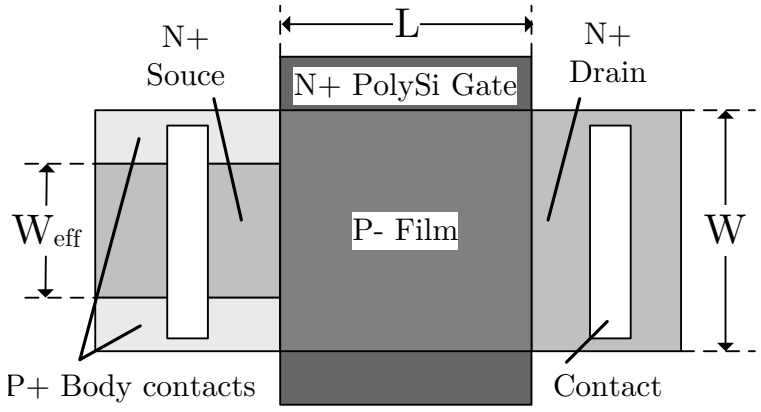

Figure 2.5: Top view of a Split-Source N-channel SOI-MOSFET (NSOI) with source-side P^+ body contacts.

The ratio of effective source width to the drain width is $W_{eff}/W \approx 0.6$. The Split-Source transistor is designed for a supply voltage of 5 V for analog circuit applications. The minimum channel length L is 1.6 µm. The film of the Split-Source P-channel SOI (PSOI) transistor is contacted with an N^+ body contact on the source side.

2.1.2 HGATE Transistor

The name of the HGATE SOI-MOSFET devices is derived from its H-shaped gate. A top view of the N-channel HGATE transistor (NHGATE) is shown in Figure 2.6. The H-shaped gate has the advantage of suppressing the sidewall leakage current, which will be discussed in Section 3.8.3. A photograph of the NHGATE device is shown in Figure 2.7.

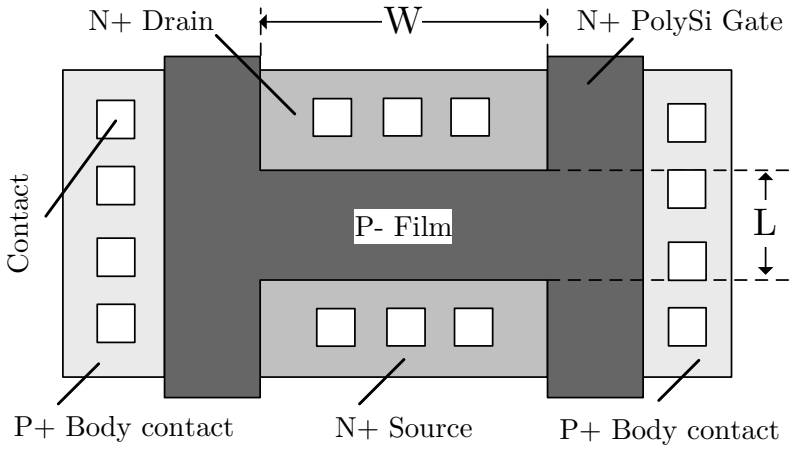

Figure 2.6: Top view of an N-channel HGATE SOI-MOSFET (NHGATE) with a P^+ body contacts on each side of the channel.

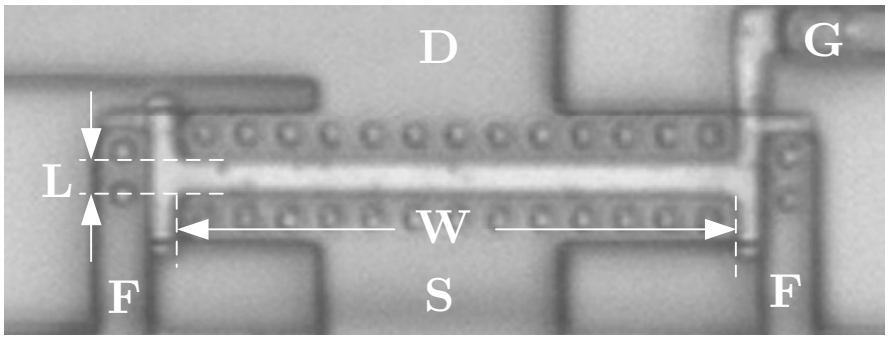

Figure 2.7: Photograph of an NHAGTE SOI-MOSFET in the considered SOI technology.

The body contact of the NHGATE is realized by P^+ implanted areas on the left hand side and right hand side of the channel. The body contacts are usually short-circuited via the metal one layer. Thereby, the effective width of the source and drain regions are equal in case of the HGATE transistor. It is a symmetrical device due to the fact that source and drain are interchangeable, which is one of the main advantages over the Split-Source NSOI/PSOI devices. The minimum

transistor length L for analog applications is 1.6 µm. The minimum width W is 3.6 µm. Effective doping concentrations of the NHGATE and PHGATE transistors are also $N_A \approx 3 \cdot 10^{16}\,\mathrm{cm}^{-3}$ and $N_D \approx 1.8 \cdot 10^{16}\,\mathrm{cm}^{-3}$, respectively.

2.1.3 PIN-Diode

In a PIN-diode, the P^+ and N^+ regions are separated by an intrinsic silicon region N_I. Figure 2.8 shows a cross section of a PIN-diode in the considered 1.0 µm SOI technology.

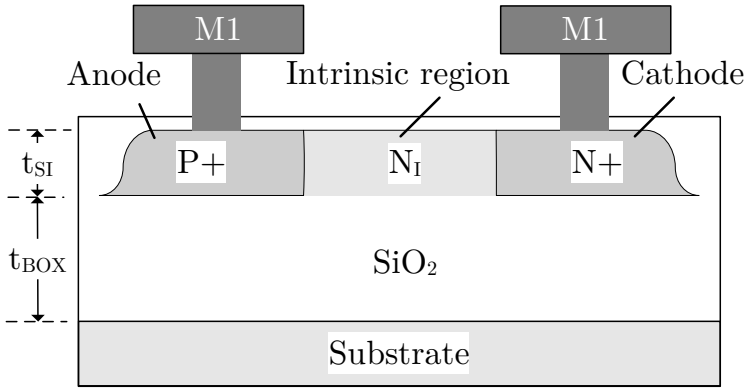

Figure 2.8: Cross section of a PIN-diode in the 1.0 µm SOI technology.

When biased in reverse direction, the space charge region (SCR) extends over the entire intrinsic region. Thereby the use of the additional intrinsic region offers improved high voltage capability [Rei07]. The reverse breakdown voltage of the PIN-diode is approximately 31 V [Dit12]. Among other applications, the PIN-diode is also used as an ESD (electrostatic discharge) protection on input- and output pads of the circuits. Since a PNP bipolar transistor is currently not available in the considered SOI technology, the PIN-diode is also used in bandgap voltage reference circuits to generate an output voltage independent on temperature and supply voltage.

2.1.4 P^+ Implanted Resistor (RPPLUS)

The P^+ implanted resistor (RPPLUS) represents a good compromise between required area and sheet resistance and is also suited for applications were good resistor device matching is required [Ver97]. A cross section of a P^+ implanted resistor is shown in Figure 2.9.

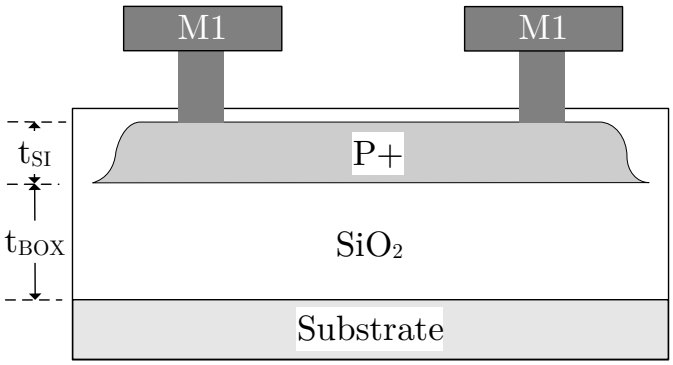

Figure 2.9: Cross section of a P^+ implanted resistor (RPPLUS) in the 1.0 µm SOI technology.

The resistor has a sheet resistance of approximately 300 Ω/□ with a first order temperature coefficient $TK_1 = 9.68 \cdot 10^{-4}\,1/\mathrm{K}$ and a second order temperature coefficient $TK_2 = 1.12 \cdot 10^{-6}\,1/\mathrm{K}^2$ [Dit12].

2.1.5 Poly-Silicon Resistor (RPOLY)

The poly-silicon resistor (RPOLY) is realized by a layer of poly-silicon deposited on field-oxide. The sheet resistance of the poly-silicon resistor is 16.8 Ω/□. The first order and second order temperature coefficients are $TK_1 = 1.41 \cdot 10^{-3}\,1/\mathrm{K}$ and $TK_2 = -1.15 \cdot 10^{-6}\,1/\mathrm{K}^2$, respectively. A cross section of the RPOLY resistor is shown in Figure 2.10.

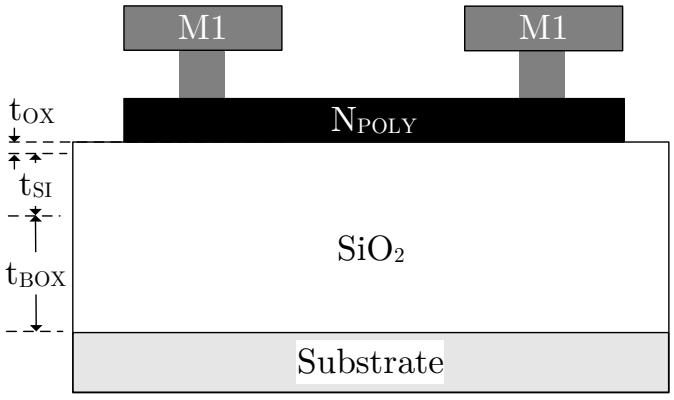

Figure 2.10: Cross section of a poly-silicon resistor (RPOLY) in the 1.0 µm SOI technology.

2.1.6 Capacitor

A poly-N^+ capacitor is composed of a poly-silicon layer over gate-oxide, forming one side of the capacitor, and an active N^+ area forming the opposite side of the capacitor plate. A cross section of the poly-N^+ capacitor can be seen in Figure 2.11.

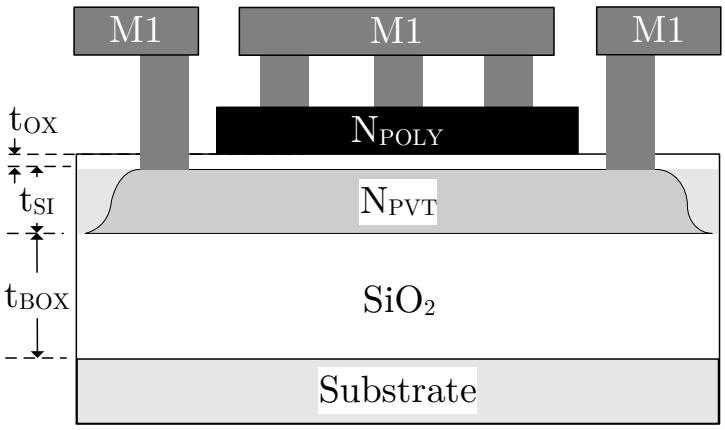

Figure 2.11: Cross section of a poly-N^+ capacitor in the 1.0 µm SOI technology.

In order to achieve a low voltage dependency of the capacitance, an doping concentration N_{PVT} is implanted into the active area of the capacitor.

Table 2.1 summarizes all process dimensions and doping concentration.

Table 2.1: Process dimensions and doping concentrations.

Symbol	Description	Value	Unit
t_{SI}	Thickness of the silicon film	150	nm
t_{ox1}	Front gate oxide thickness	40	nm
t_{BOX}	Back gate oxide (buried oxide) thickness	400	nm
W_{eff}	Effective channel width in Split-Source SOI MOSFETs	$\approx 0.6 \cdot$ W	nm
N_A	Effective channel surface doping concentration for n-channel SOI-MOSFETs	$3 \cdot 10^{16}$	cm^{-3}
N_D	Effective channel surface doping concentration for p-channel SOI-MOSFETs	$1.8 \cdot 10^{16}$	cm^{-3}
N_{Sub}	Effective substrate (back gate) N^- doping concentration	$1 \cdot 10^{14}$	cm^{-3}

Chapter 3

Fundamentals of SOI-MOSFETs

In this chapter, fundamental SOI-MOSFET device physics are presented in order to prepare the discussion on the SOI-MOSFET device characteristics at high temperatures in the following chapters. Fundamental device parameters, e.g. threshold voltage and leakage current are described from a theoretical perspective, and their dependencies on temperature are experimentally evaluated in Chapter 4.

3.1 Carrier Concentration at Thermal Equilibrium

In an intrinsic silicon semiconductor, the number of atoms in the crystal lattice is approximately $5 \cdot 10^{22}\,\text{atoms/cm}^3$ [TM11]. At absolute zero temperature (0 K), all electrons are bound to the atom's nucleus and their net charge is canceled [TM11]. Due to vibration of the crystal lattice at higher temperatures, some of the electrons gain enough energy to become unbound. If an electron escapes its bound, it leaves a positive charge behind. Positive charges are thereby created by the vacancy of an electron and are referred to as *holes*. Holes are considered free charges because neighbor valence electrons can fill the bound, leaving another electron vacancy behind [TM11]. As electrons and holes move through the crystal lattice, they can recombine in one place. The creation of free charge carriers in silicon can be described best by the energy band structure of solids. In silicon, electrons are bound to their valence neighbors and have a potential energy not larger than E_v, called the valence band energy [TM11]. Free electrons are created, if an electron gains the energy E_G, referred to as the bandgap energy, to reach the conduction band energy E_C.

$$E_G = E_C - E_V \tag{3.1}$$

The bandgap energy of silicon at absolute zero temperature is $E_G(0) = 1.17\,\text{eV}$ [SN07]. At temperatures higher than 0 K, vibration of the crystal lattice can provide enough energy to set a small concentration of electrons n free, also creating a free holes concentration p. Since every free electron also creates one free hole, the concentration of free electrons and holes is equal, the so called intrinsic carrier concentration n_i [SN07].

$$n = p = n_i \tag{3.2}$$

The intrinsic carrier concentration n_i as a function of temperature can be written as [Col04]

$$n_i = 3.9 \cdot 10^{16} \cdot T^{3/2} \cdot exp\left(\frac{-E_G(0)}{2kT}\right) , \tag{3.3}$$

in which k is the Boltzmann constant $k = 8.617 \cdot 10^{-5}\,\frac{\text{eV}}{\text{K}}$ and T is the temperature in Kelvin. The number of free electrons and holes in a semiconductor can be controlled by implanting atoms other than silicon into the silicon crystal lattice [TM11]. Implanted or doped semiconductors are called *extrinsic* semiconductors. The number of free electrons n_0 in n-type doped semiconductors is mainly determined by the impurity concentration N_D. Due to recombination of electrons and holes, the number of free holes decreases when the n-type doping concentration increases. Their product is the same as in the intrinsic case [SN07].

$$n_0 \cdot p_0 = n_i^2 \tag{3.4}$$

The number of dopant atoms N_D in an extrinsic semiconductor is several orders of magnitude higher than the number of free carriers in the intrinsic semiconductor. Thus, the number of free electrons n_0 is approximately equal to the number of dopant atoms N_D [SN07].

$$n_0 \approx N_D \tag{3.5}$$

Combining Equations (3.4) and (3.5), the number of free holes p_0 is given by

$$p_0 = \frac{n_i^2}{N_D} . \tag{3.6}$$

In analogy, the number of free holes and electrons in a p-type semiconductor with a doping concentration N_A is given by Equations (3.7) and (3.8) [SN07].

$$p_0 \approx N_A \tag{3.7}$$

$$n_0 = \frac{n_i^2}{N_A} \tag{3.8}$$

The relationship between the number of free charge carriers, doping concentration and temperature can be derived from the Fermi-Dirac distribution function $F(E)$ shown in Equation (3.9) [SN07].

$$F(E) = \frac{1}{1 + exp\left[(E - E_F)/kT\right]} \tag{3.9}$$

The distribution describes the probability that an energy level E is occupied by an electron. In an intrinsic semiconductor, the Fermi level E_F is defined as the intrinsic Fermi level E_i. In case of doped n-type silicon, E_F is larger than E_i, whereby in case of p-type silicon E_F is smaller than E_i. The electron and hole concentrations of a semiconductor can then be expressed by Equations (3.10) and (3.11) [SN07], respectively.

$$n_0 = n_i \cdot exp\left(\frac{E_F - E_i}{kT}\right) = n_i \cdot exp\left(-\frac{\phi_F}{V_t}\right) \tag{3.10}$$

$$p_0 = n_i \cdot exp\left(\frac{E_i - E_F}{kT}\right) = n_i \cdot exp\left(\frac{\phi_F}{V_t}\right) \tag{3.11}$$

In Equations (3.10) and (3.11), V_t is the thermal voltage given by $V_t = kT/q$ and ϕ_F is the Fermi potential, which can be written as

$$\phi_F = \frac{E_i - E_F}{q} \,. \tag{3.12}$$

In an extrinsic semiconductor, n_0 equals approximately the number of doping atoms N_D and p_0 equals approximately N_A. The Fermi potentials for n-type and p-type semiconductors are given in Equations (3.13) and (3.14) [SN07].

$$\phi_{Fn} \approx -V_t \cdot ln\left(\frac{N_D}{n_i}\right) \tag{3.13}$$

$$\phi_{Fp} \approx V_t \cdot ln\left(\frac{N_A}{n_i}\right) \tag{3.14}$$

3.2 Depletion States and Surface Potentials

The absence of free charge carriers, i.e. electrons and holes in a semiconductor region is known as a depletion region or space charge region (SCR). In this section,

the depletion states of the silicon film as well as the surface potentials in SOI-MOSFETs are developed and discussed. A cross section of the SOI-MOSFET in x direction is shown in Figure 3.1. The front gate surface, i.e. the interface of front gate oxide and silicon channel is considered 0 in x direction, whereby x increases going deeper into the silicon film. The transistor device consists of a Metal-Oxide-Semiconductor-Oxide-Semiconductor structure. The depletion regions x_{d1} and x_{d2} are dependent on the surface potentials ϕ_{S1} (defined at $x = 0$) and ϕ_{S2} (defined at $x = t_{SI}$) and thereby on the front gate voltage V_{G1} and the back gate voltage V_{G2}.

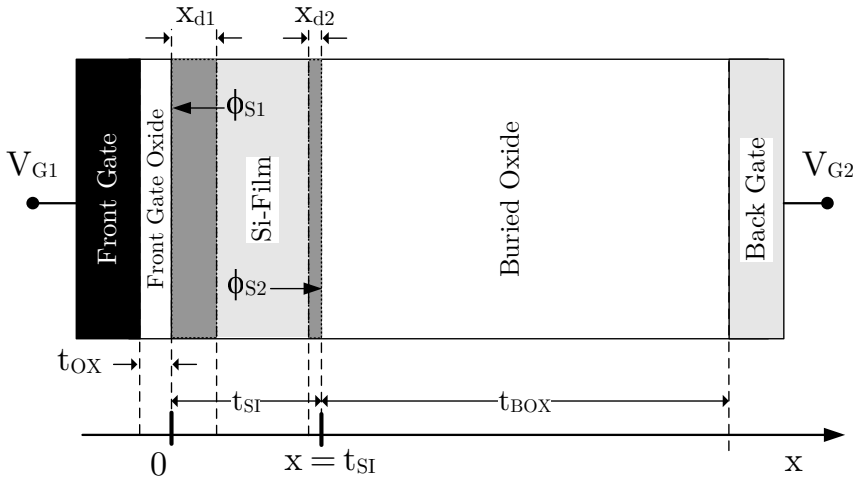

Figure 3.1: Metal-Oxide-Semiconductor-Oxide-Semiconductor structure.

Two basic depletion states of the SOI-MOSFET are distinguished:

Partially depleted (PD): The sum of the front gate depletion region x_{d1} and back gate depletion region x_{d2} is smaller than the silicon film thickness t_{SI}. In this case, an electrically neutral region called *body* is present in the silicon film. Figure 3.2 shows an SOI-MOSFET with a partially depleted silicon film and a neutral body region.

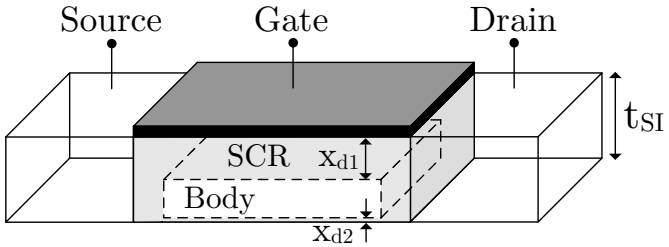

Figure 3.2: Partially depleted (PD) SOI-MOSFET with a neutral body region.

$$(x_{d1} + x_{d2}) < t_{SI} \tag{3.15}$$

Fully depleted (FD): The sum of the front gate depletion region x_{d1} and back gate depletion region x_{d2} is equal to, or greater than the silicon film thickness t_{SI}. The two depletion regions overlap and the silicon film is fully depleted. Figure 3.3 shows an SOI-MOSFET with a fully depleted silicon film.

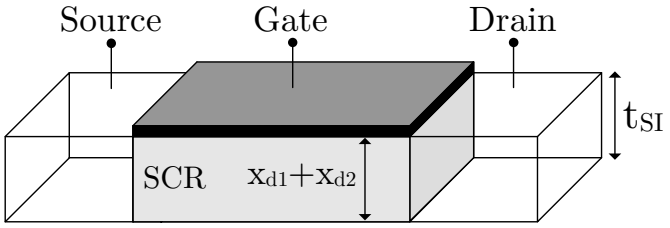

Figure 3.3: Fully depleted (FD) SOI-MOSFET.

$$(x_{d1} + x_{d2}) \geq t_{SI} \tag{3.16}$$

The silicon film changes from one depletion state to the other, dependent on the front gate voltage V_{G1}, back gate voltage V_{G2}, drain-source voltage V_{DS} and temperature T. This can cause the coexistence of partially depleted and fully depleted devices within a single process and even within a single circuit. For that reason, dynamically depleted (DD) transistors have to be considered for analog circuit design in a wide temperature range.

Dynamically depleted (DD): The depletion state of the silicon film dynamically changes from fully depleted to partially depleted or vice versa, depending on the bias conditions of V_{G1} and V_{G2}, drain-source voltage V_{DS} and temperature T.

3.2.1 Partially depleted Devices

In this section, expressions for the depletion regions x_{d1} and x_{d2}, as well as the surface potentials ϕ_{S1} and ϕ_{S2} in a partially depleted SOI-MOSFET are derived from basic device equations. These expressions are required for the calculation of the threshold voltage later on. Figure 3.1 can be used as an illustration of a partially depleted silicon film, whereby N-channel devices are considered in the following analysis. If the non-depleted silicon film between the depletion regions

x_{d1} and x_{d2} is considered grounded, the front gate interface and the back gate interface can be discussed separately [Col04].

The depletion charge per unit area within the depletion region x_{d1} is Q'_d and the gate oxide capacitance per unit area is C'_{OX1}. The surface potential beneath the front gate oxide is ϕ_{S1} and the front gate voltage is V_{G1} [Hu10].

$$V_{G1} = V_{FB1} + \phi_{S1} - \frac{Q'_d}{C'_{OX1}} \tag{3.17}$$

In Equation (3.17), V_{FB1} is the flatband voltage for which the space charge inside the silicon film is zero. Neglecting charges in the front gate oxide, the flatband voltage V_{FB1} is equal to the metal-semiconductor work function difference ϕ_{ms1}.

$$V_{FB1} = \phi_{ms1} \tag{3.18}$$

The metal-semiconductor work function difference ϕ_{ms1} is given by Equation (3.19) [SN07].

$$\phi_{ms1} = \phi_m - \phi_s = \phi_m - \left[\chi_{SI} + \frac{E_g}{2q} + \phi_F\right] \tag{3.19}$$

Depending on whether N-channel or P-channel device are considered, ϕ_F in Equation (3.19) has to be replaced by ϕ_{Fp} or ϕ_{Fn}, respectively. In (3.19), ϕ_m is the work function of the poly-silicon gate, ϕ_s the work function of the semiconductor and $\chi_{SI} = 4.05\,\mathrm{V}$ is the electron affinity of silicon [SN07]. For an N^+ poly-silicon gate with a P^- semiconductor film, ϕ_{ms1} and thereby also the flatband voltage V_{FB1} at room temperature is approximately $-1.1\,\mathrm{V}$ [SN07].

The depletion charge per unit area Q'_d as a function of surface potential ϕ_{S1} can be derived from the Poisson equation and is discussed in detail in [TM11]. The depletion charge in N-channel devices as a function of the front gate surface potential $Q'_d(\phi_{S1})$ is given in Equation (3.20) [TM11].

$$Q'_d(\phi_{S1}) = -\mathrm{sgn}(\phi_{S1})\sqrt{2q\epsilon_{si}N_A}\sqrt{V_t\, e^{-\phi_{S1}/V_t} - V_t + \phi_{S1}} \tag{3.20}$$

In (3.20), $\mathrm{sgn}(\phi_{S1})$ is the signum function, which is equal to -1 for $\phi_{S1} < 0$, 0 for $\phi_{S1} = 0$ and 1 for $\phi_{S1} > 0$. In case of depletion, the surface potential ϕ_{S1} is above zero but smaller than ϕ_F [SN07]. In order to simplify the expression, the exponential term in (3.20) and the thermal voltage V_t are neglected. The depletion charge per unit area $Q'_d(\phi_{S1})$ can be rewritten as [TM11]

$$Q'_d(\phi_{S1}) \approx -\sqrt{2q\epsilon_{si}N_A}\sqrt{\phi_{S1}}\ . \tag{3.21}$$

With (3.21), Equation (3.17) can be rewritten to

$$V_{G1} = V_{FB1} + \phi_{S1} + \frac{\sqrt{2q\epsilon_{si}N_A}}{C'_{OX1}}\sqrt{\phi_{S1}}\ . \tag{3.22}$$

The coefficient of $\sqrt{\phi_{S1}}$ in the last term is the so called *body-effect coefficient* and is given by [TM11]

$$\gamma_1 = \frac{\sqrt{2q\epsilon_{si}N_A}}{C'_{OX1}}\ . \tag{3.23}$$

The relationship between the front gate voltage V_{G1} and the surface potential ϕ_{S1} in Equation (3.22) can now be solved for the surface potential. Using the substitution $x = \sqrt{\phi_{S1}}$, Equation (3.22) can be rewritten as

$$0 = V_{FB1} + x^2 + \gamma_1 x - V_{G1}\ . \tag{3.24}$$

Solving (3.24) for x and re-substituting $\phi_{S1} = x^2$ yields the surface potential ϕ_{S1} as a function of front gate voltage V_{G1} and flatband voltage V_{FB1} [Jes10] [TM11]

$$\phi_{S1} = \left[-\frac{\gamma_1}{2} + \sqrt{\left(\frac{\gamma_1}{2}\right)^2 + V_{G1} - V_{FB1}}\right]^2\ . \tag{3.25}$$

Using Equation (3.25), the surface potential ϕ_{S1} can now be calculated for a given front-gate voltage V_{G1}. Analogously, the surface potential ϕ_{S2} can be calculated by replacing γ_1 with $\gamma_2 = \sqrt{2q\epsilon_{si}N_A}/C'_{OX2}$, V_{G1} with V_{G2} and V_{FB1} with V_{FB2}.

The depletion depth x_{d1} of a metal-oxide-semiconductor (MOS) structure for a given surface potential ϕ_{S1} and doping concentration N_A is given by Equation (3.26) [SN07].

$$x_{d1} = \sqrt{\frac{2\epsilon_{si}}{qN_A}}\sqrt{\phi_{S1}} = \sqrt{\frac{2\epsilon_{si}\phi_{S1}}{qN_A}} \tag{3.26}$$

Combining (3.25) with (3.26), the depletion depths x_{d1} and x_{d2} of a partially depleted SOI-MOSFET are given by Equations (3.27) and (3.28), respectively.

$$x_{d1} = \sqrt{\frac{2\epsilon_{si}}{qN_A}}\left[-\frac{\gamma_1}{2} + \sqrt{\left(\frac{\gamma_1}{2}\right)^2 + V_{G1} - V_{FB1}}\right] \tag{3.27}$$

$$x_{d2} = \sqrt{\frac{2\epsilon_{si}}{qN_A}} \left[-\frac{\gamma_2}{2} + \sqrt{\left(\frac{\gamma_2}{2}\right)^2 + V_{G2} - V_{FB2}} \right] \tag{3.28}$$

In case both gate voltages V_{G1} and V_{G2} are zero, the depletion regions x_{d1} and x_{d2} are mainly dependent on the flatband voltages V_{FB1} and V_{FB2}. Thereby, both depletion regions are dependent on temperature and doping concentration. When the SOI-MOSFET device is turned off by an applied gate-source voltage of $V_{GS} = 0\,\mathrm{V}$, the channel doping concentration and the temperature determine whether the device is fully depleted or partially depleted. Both depletion depths x_{d1} and x_{d2} over channel doping concentration and temperature are shown in Figure 3.4.

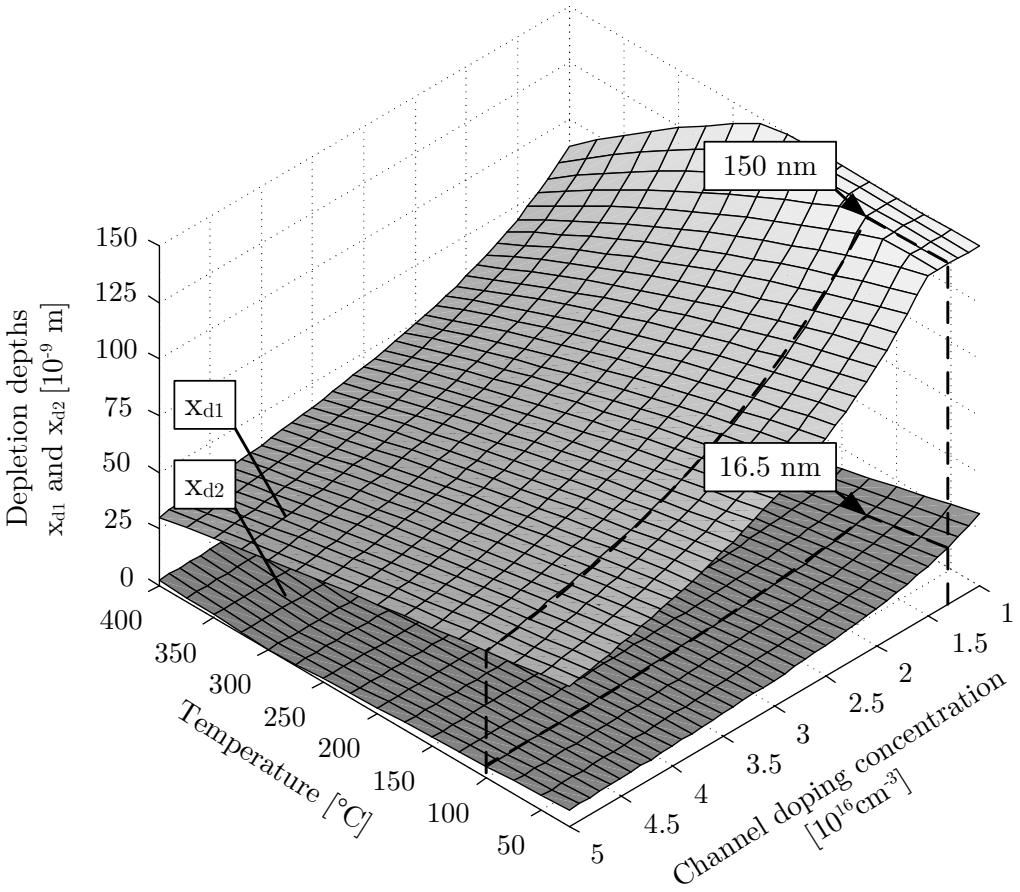

Figure 3.4: Depletion depths x_{d1} and x_{d2} with a front gate voltage of $V_{G1} = 0\,\mathrm{V}$ and back gate voltage $V_{G2} = 0\,\mathrm{V}$ over temperature and channel doping concentration.

Neglecting oxide charges, the flatband voltage of the back gate interface V_{FB2} can be calculated using Equation (3.29).

$$\begin{aligned} V_{FB2} &= \phi_{ms2} = \phi_{s_{BG}} - \phi_{s_{Film}} \\ &= \left[\chi_{SI} + \frac{E_g}{2q} + \phi_{F_{BG}}\right] - \left[\chi_{SI} + \frac{E_g}{2q} + \phi_{F_{Si}}\right] \\ &= \phi_{F_{BG}} - \phi_{F_{Si}} \end{aligned} \tag{3.29}$$

For the calculation of V_{FB2} in Equation (3.29), an N^- substrate doping concentration of $N_{Sub} = 1 \cdot 10^{14}\,\mathrm{cm}^{-3}$ has been assumed. Due to the thick back gate oxide, the depletion depth x_{d2} at the back interface is smaller compared to the front depletion depth x_{d1}. For a silicon film doping concentration of $1.3 \cdot 10^{16}\,\mathrm{cm}^{-3}$ and a temperature of 100 °C, the depletion depth x_{d1} is 150 nm and x_{d2} is 16.5 nm. At high temperatures, the back gate depletion depth x_{d2} can be neglected and the front gate depletion depth x_{d1} drops below 100 nm.

3.2.2 Fully depleted Devices

The device is fully depleted when $(x_{d1} + x_{d2}) \geq t_{SI}$. In that case, the surface potentials ϕ_{S1} and ϕ_{S2} can no longer be considered independent from each other. The relationship between both potentials, the front gate voltage V_{G1} and back gate voltage V_{G2} can be described by Equations (3.30) and (3.31) [Col04] [HF83].

$$V_{G1} = \phi_{ms1} - \frac{Q_{ox1}}{C_{OX1}} + \phi_{S1}\left(1 + \frac{C_{si}}{C_{OX1}}\right) - \phi_{S2}\frac{C_{si}}{C_{OX1}} - \frac{Q'_d}{2C'_{OX1}} \tag{3.30}$$

$$V_{G2} = \phi_{ms2} - \frac{Q_{ox2}}{C_{OX2}} + \phi_{S2}\left(1 + \frac{C_{si}}{C_{OX2}}\right) - \phi_{S1}\frac{C_{si}}{C_{OX2}} - \frac{Q'_d}{2C'_{OX2}} \tag{3.31}$$

In Equations (3.30) and (3.31), Q_{ox1} and Q_{ox2} are the front gate and back gate oxide charges, C_{OX2} is the back gate capacitance, C'_{OX2} is the back gate capacitance per unit area, C_{si} is the depletion capacitance and Q'_d is here the depletion charge per unit area of the fully depleted silicon film. Charge sharing between the front gate and the back gate has been considered, by dividing the depletion charge per unit area Q'_d in the last terms of (3.30) and (3.31) by a factor of 2. This value can vary, depending on the back gate bias condition [Col04]. To obtain the front gate surface potential ϕ_{S1} as a function of V_{G1} and V_{G2} similarly to the analysis of partially depleted SOI-MOSFETs, Equations (3.30) and (3.31) have to be solved for ϕ_{S1} and ϕ_{S2}, whereby oxide charges are neglected for simplicity.

$$\phi_{S1}\left(1+\frac{C_{si}}{C_{OX1}}\right)=V_{G1}-\phi_{ms1}+\phi_{S2}\frac{C_{si}}{C_{OX1}}+\frac{Q'_d}{2C'_{OX1}} \tag{3.32}$$

$$\phi_{S2}\left(1+\frac{C_{si}}{C_{OX2}}\right)=V_{G2}-\phi_{ms2}+\phi_{S1}\frac{C_{si}}{C_{OX2}}+\frac{Q'_d}{2C'_{OX2}} \tag{3.33}$$

Inserting (3.33) in (3.32) and solving (3.32) for ϕ_{S1} yields the front gate surface potential of a fully depleted SOI-MOSFET, given by

$$\begin{aligned}\phi_{S1} \;=\; & \left[1+\frac{C_{si}C_{OX2}}{C_{OX1}\left(C_{si}+C_{OX2}\right)}\right]^{-1}\left[V_{G1}-\phi_{ms1}+\frac{Q'_d}{2C'_{OX1}}+\right.\\ & \left.+\frac{C_{si}C_{OX2}}{C_{OX1}\left(C_{OX2}+C_{si}\right)}\left(V_{G2}-\phi_{ms2}+\frac{Q'_d}{2C'_{OX2}}\right)\right]\,.\end{aligned} \tag{3.34}$$

In analogy, the back gate surface potential ϕ_{S2} in a fully depleted SOI-MOSFET is given by

$$\begin{aligned}\phi_{S2} \;=\; & \left[1+\frac{C_{si}C_{OX1}}{C_{OX2}\left(C_{si}+C_{OX1}\right)}\right]^{-1}\left[V_{G2}-\phi_{ms2}+\frac{Q'_d}{2C'_{OX2}}+\right.\\ & \left.+\frac{C_{si}C_{OX1}}{C_{OX2}\left(C_{OX1}+C_{si}\right)}\left(V_{G1}-\phi_{ms1}+\frac{Q'_d}{2C'_{OX1}}\right)\right]\,.\end{aligned} \tag{3.35}$$

Figure 3.5 shows the surface potentials ϕ_{S1} and ϕ_{S2} in fully depleted condition as well as the qualitative potential distribution ϕ_x.

The potential distribution $\phi(x)$ can be calculated solving the one dimensional Poisson equation, i.e. by integrating Equation (3.36) twice [Col04].

$$\frac{d^2\phi(x)}{dx^2}=\frac{qN_{CH}}{\epsilon_{si}} \tag{3.36}$$

By applying the boundary conditions from Equations (3.34) and (3.35), the potential distribution is then given by

$$\phi(x)=\frac{qN_{CH}}{2\epsilon_{si}}x^2+\left(\frac{\phi_{S2}-\phi_{S1}}{t_{SI}}-\frac{qN_{CH}t_{SI}}{2\epsilon_{si}}\right)x+\phi_{S1}\,. \tag{3.37}$$

This expression is especially useful for the calculation of the potential distribution across the silicon film for given surface potentials and will be used later on. In a fully depleted silicon film, the depletion charge per unit area Q'_d is determined by the film thickness t_{SI} and is given by (3.38) [Col04].

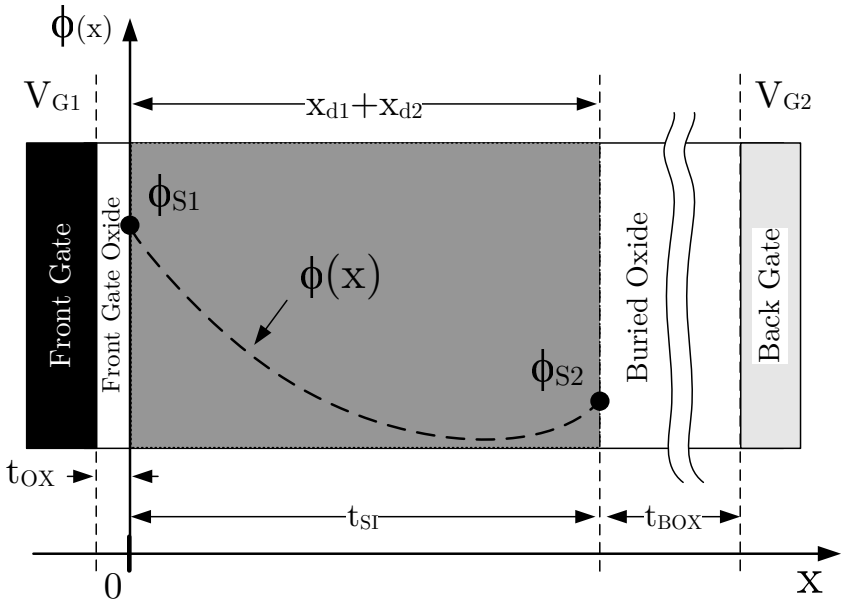

Figure 3.5: Qualitative characteristic of the surface potentials ϕ_{S1} and ϕ_{S2} and the potential across the silicon film $\phi(x)$ in a fully depleted SOI-MOSFET.

$$Q'_d = -qN_{CH}t_{SI} \tag{3.38}$$

In the fully depleted device, the depletion charge Q'_d is independent on temperature, which is an important difference between partially depleted and fully depleted SOI-MOSFETs [Col04]. It affects most of the SOI-MOSFET's analog characteristics, as we will see in the following sections.

3.3 Body factor

The body factor n describes the coupling of front gate voltage V_{G1} and the surface potential ϕ_{S1}. The body factor is thereby an important analog parameter to determine the effectiveness of channel control by the front gate of the transistor. It is defined as [Col04]

$$n = \left(\frac{d\phi_{S1}}{dV_{G1}}\right)^{-1}. \tag{3.39}$$

In weak inversion, the slope of the logarithmic channel current as a function of V_{GS} is equal to $1/n$, whereby small values of n are preferred for a high weak inversion slope [Col04]. Expressions for the front gate surface potential and the back gate surface potential in PD and FD mode were developed in Sections 3.2.1

and 3.2.2, respectively. In this section, the expression for the body factor n will be derived from these expressions.

The relationship between the surface potential and the front gate voltage of a partially depleted transistor was given by Equation (3.17). To obtain n in partially depleted mode, this expression can be rearranged and differentiated once with respect to ϕ_{S1}.

$$n|_{PD} = \left(\frac{d\phi_{S1}}{dV_{G1}}\right)^{-1} = \frac{dV_{G1}}{d\phi_{S1}} = \frac{d}{d\phi_{S1}}\left(V_{FB1} + \phi_{S1} - \frac{Q'_d}{C'_{OX1}}\right) \tag{3.40}$$

When the depletion capacitance is defined as $C'_D = -dQ'_d/d\phi_{S1} = \epsilon_{si}/x_{d1}$ [TM11], n can be written as

$$n|_{PD} = \frac{d}{d\phi_{S1}}\left(V_{FB1} + \phi_{S1}\right) + \frac{C'_D}{C'_{OX1}} = 1 + \frac{C'_D}{C'_{OX1}} = 1 + \frac{\epsilon_{si}}{x_{d1}C'_{OX1}}\,. \tag{3.41}$$

In fully depleted mode, the body factor n can be obtained from solving Equation (3.34) for V_{GS1}, followed by the differentiation after ϕ_{S1}. Oxide charges are neglected in this analysis. For the fully depleted condition, $n|_{FD}$ then results in

$$n|_{FD} = 1 + \frac{C_{si}C_{OX2}}{C_{OX1}\left(C_{si} + C_{OX2}\right)}\,. \tag{3.42}$$

In the considered SOI technology, $n|_{FD}$ is 1.09 whereby $n|_{PD}$ can vary between 1.1 and 10, depending on the depletion depth x_{d1}. For a more compact form, Equation (3.34) can be rewritten as

$$\begin{aligned}\phi_{S1} = \quad & \frac{1}{n|_{FD}}\left[V_{G1} - \phi_{ms1} + \frac{Q'_d}{2C'_{OX1}} + \right. \\ & \left. + \left(n|_{FD} - 1\right)\left(V_{G2} - \phi_{ms2} + \frac{Q'_d}{2C'_{OX2}}\right)\right]\,.\end{aligned} \tag{3.43}$$

This expression is very useful to determine the front surface potential of fully depleted SOI-MOSFETS, for a given front gate voltage and back gate voltage.

3.4 Subthreshold Swing

The subthreshold swing S is defined as the inverse slope of the logarithmic drain current $I_d\left(V_{GS}\right)$ in the weak inversion region of the transistor. It determines,

how much change in gate voltage is required in order to increase the drain current by one order of magnitude (one decade). It is expressed in mV/decade, whereby small values are preferred. The expression for the subthreshold slope can be derived from the weak inversion current and is explained in detail in [Col04][Col86][RLR+99][RKC+02], whereby interface traps are neglected in this analysis.

$$S = \frac{dV_{GS}}{d\left(logI_d\right)} = V_t \cdot n \cdot ln\left(10\right) \tag{3.44}$$

In Equation (3.44), n is the body factor derived in the preceding section for partially depleted and fully depleted SOI-MOSFETs. If fully depleted SOI-MOSFETs are considered, the subthreshold swing can be written as

$$S|_{FD} = V_t \left(1 + \frac{C_{si}C_{OX2}}{C_{OX1}\left(C_{si} + C_{OX2}\right)}\right) ln\left(10\right) \ . \tag{3.45}$$

In partially depleted SOI-MOSFETs, $S|_{PD}$ is written as [Col04]

$$S|_{PD} = V_t \left(1 + \frac{\epsilon_{si}}{x_{d1}C'_{OX1}}\right) ln\left(10\right) \ . \tag{3.46}$$

In a fully depleted SOI-MOSFET with a body factor of $n = 1.09$, the subthreshold swing at room temperature is approximately 64 mV/decade, whereby in a partially depleted SOI-MOSFET, S is typically larger than 100 mV/decade. The subthreshold swings of partially depleted SOI-MOSFETs and fully depleted SOI-MOSFETs calculated using Equations (3.45) and (3.46) are shown over temperature in Figure 3.6.

It can be seen that the increase of subthreshold swing for fully depleted devices is small and caused by the linear increase of the thermal voltage V_t with temperature. For partially depleted devices, the subthreshold swing strongly increases at high temperatures due to variation of the body factor n. The decreased subthreshold swing in fully depleted SOI-MOSFETs is a major performance advantage over partially depleted SOI-MOSFETs and results in a higher weak inversion transconductance, as it will be presented in Section 3.10.

3.5 PN-Junctions

3.5.1 Built-In Potential

A PN-junction is formed when an n-type semiconductor region is joined with a p-type semiconductor region. Due to charge diffusion mechanisms inside the

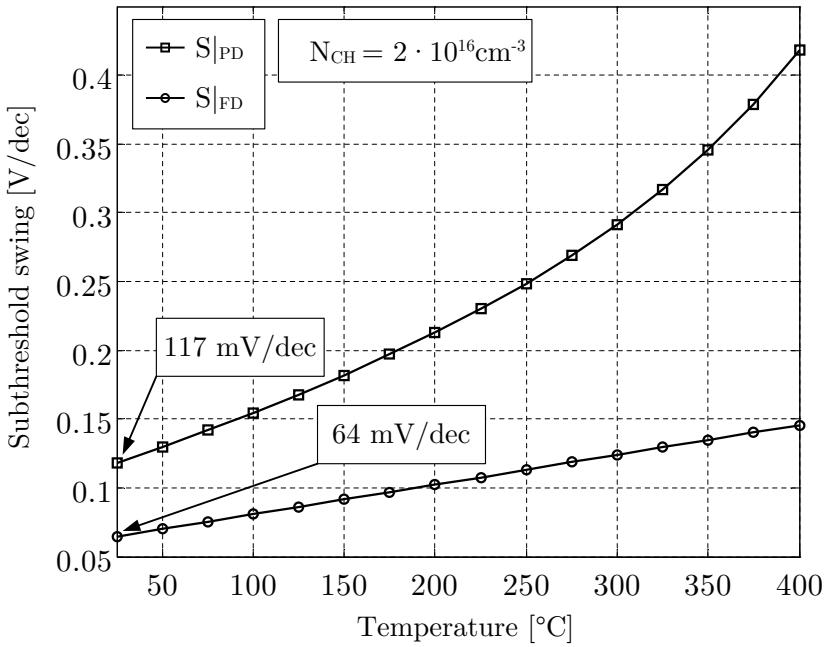

Figure 3.6: Calculated subthreshold swing $S|_{FD}$ of fully depleted SOI-MOSFETs and $S|_{PD}$ of partially depleted SOI-MOSFETs over temperature.

semiconductor, a depletion region or space charge region is formed at the interface of both regions. A built-in potential ϕ_{bi}, equal to the potential across the depletion region is established between the two semiconductor regions. The built-in potential can be calculated by the difference in Fermi potentials of the two semiconductors [TM11] [Hu10].

$$\phi_{bi} = \phi_{Fp} - \phi_{Fn} = V_t \, ln \left(\frac{N_D N_A}{n_i^2} \right) \tag{3.47}$$

Once ϕ_{bi} is established, electrons in the n-region and holes in the p-region cannot easily cross the junction. If we consider the PN-junction between the silicon film and source region in an N-channel SOI-MOSFET, shown in Figure 3.7, this effect can cause the accumulation of generated holes at the point of the lowest potential inside the undepleted silicon film and is thereby responsible for floating body effects [PFW+03b].

If a forward bias is applied to the PN-junction, the potential across the junction decreases by the value of the forward bias and the potential barrier is reduced. If a back-bias is applied on the other hand, the voltage across the PN-junction increases by the value of the back-bias and the potential barrier for holes and electrons increases [SN07]. At this point, special attention should be paid to the

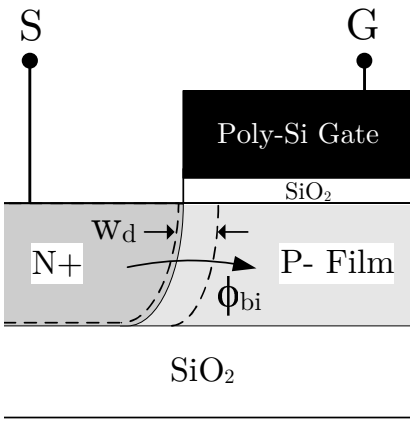

Figure 3.7: Cross section of the PN-junction at the interface between film and source in an N-channel SOI-MOSFET with depletion width w_d and built-in potential ϕ_{bi}.

forward bias condition. A forward bias will lower the potential barrier between the silicon film and the source region. In this case, generated holes in the film can easily enter the source region. Thus, an accumulation of majority carriers in the film can be decreased by a forward bias of the film-source PN-junction [PFW+03b]. It will be shown in the next section, how the surface potential ϕ_{S1} contributes to the forward bias of the film-source PN-junction in fully depleted SOI-MOSFETs.

3.5.2 Built-In Potential Lowering

The built-in potential of the film-source PN-junction was discussed in the previous section. One of the main differences between fully depleted and partially depleted SOI-MOSFETs is the existence of a *built-in potential lowering* ΔV_{bi} in FD transistors [PFW+03b]. The built-in potential lowering ΔV_{bi} is also used in the BSIMSOI simulation model in order to determine, whether the device is partially depleted or fully depleted [BSI03]. If we consider a potential distribution across the silicon film in a fully depleted device, as it was shown in Figure 3.5, the positive potential at each point x across the film-source PN-junction can be considered as a forward bias of the PN-junction. The built-in potential lowering ΔV_{bi} is usually defined at the back-interface, as a floating body is also expected at the back-interface in fully depleted mode [PFW+03b]. The built-in potential lowering ΔV_{bi} in case of a fully depleted transistor is then equal to the back gate surface potential ϕ_{S2}.

The built-in potential lowering can then be calculated by solving Equation (3.33) for ϕ_{S2}.

$$\begin{aligned}\Delta V_{bi} &= \phi_{S2}|_{FD} = \frac{C_{OX2}}{C_{OX2}+C_{si}}\left(V_{G2}-\phi_{ms2}\right)+\phi_{S1}\frac{C_{si}}{C_{OX2}+C_{si}}+\frac{Q_d}{2\left(C_{OX2}+C_{si}\right)} \\ &= \frac{C_{si}}{C_{OX2}+C_{si}}\left(\phi_{S1}+\frac{Q_d}{2C_{si}}\right)+\frac{C_{OX2}}{C_{OX2}+C_{si}}\left(V_{G2}-\phi_{ms2}\right) \end{aligned} \tag{3.48}$$

With $Q_d = -qN_{CH}t_{SI}WL$, the built-in potential lowering can be rewritten as

$$\Delta V_{bi} = \frac{C_{si}}{C_{OX2}+C_{si}}\left(\phi_{S1}-\frac{qN_{CH}t_{SI}^2}{2\epsilon_{si}}\right)+\frac{C_{OX2}}{C_{OX2}+C_{si}}\left(V_{G2}-\phi_{ms2}\right)\ . \tag{3.49}$$

In Equation (3.49), ΔV_{bi} is consistent with the expression used in [CSW+04], if DIBL (Drain Induced Barrier Lowering) and SCE (Short-Channel Effects) are neglected. It is also consistent with the expressions from [HCA+94] and [PFW+03b], if a large buried oxide thickness, and therefore $C_{OX2} \rightarrow 0$, is considered. The simplified expression can then be written as

$$\Delta V_{bi} = \phi_{S1} - \frac{qN_{CH}t_{SI}^2}{2\epsilon_{si}}\ . \tag{3.50}$$

Since the buried oxide in the considered SOI technology is equal to $t_{BOX} = 400\,\text{nm}$, the more accurate expression in (3.49) will be used in this work.

3.5.3 Depletion Width

Since the doping concentration of the silicon film is low compared to the source- and drain doping concentrations, the depletion width w_d of the PN-junction almost entirely extends into the silicon film [SN07]. The depletion width can then be calculated using Equation (3.51) [SN07][TM11].

$$w_d = \sqrt{\frac{2\epsilon_{si}}{qN_{CH}}\left(V_{bi}-V_B\right)} \tag{3.51}$$

In (3.51), V_B is the applied bias across the junction. One can see that the depletion width decreases with an applied forward bias at the film region ($V_B > 0\,\text{V}$), whereby it widens with an applied reverse bias ($V_B < 0\,\text{V}$). With a film doping concentration of $1 \cdot 10^{16}\,\text{cm}^{-3}$ and without an applied bias ($V_B = 0\,\text{V}$), the depletion width is approximately 353 nm at 25 °C and 264 nm at 350 °C. If a reverse bias of $V_B = -1\,\text{V}$ is applied, the depletion width extends to 506 nm at 25 °C and 485 nm at 350 °C. Long channel devices in the range of 5 µm are typically used for analog circuit design. It is thereby expected that the depletion

widths on source and drain junctions are not wide enough to deplete the entire channel of a long channel device. Thus, the depletion widths at the source- and drain side will be neglected in the closer examination of the depletion conditions in long channel SOI-MOSFETs. Nevertheless, they have to be considered for short channel devices.

3.6 Threshold Voltage of SOI-MOSFETs

The threshold voltage of an SOI-MOSFET device refers to the applied gate-source voltage, at which a conducting channel is formed beneath the gate of the transistor. The threshold voltage is defined in the moderate inversion region of the device where $2\phi_F < \phi_{S1} < 2\phi_F + \Delta\phi$ [TM11]. $\Delta\phi$ can be in the range of $0 \ldots 7V_t$ [TM11]. The different regions are depletion, weak inversion, moderate inversion and strong inversion.

$$\phi_{S1} = \begin{cases} 0 \ldots \phi_F & \text{in depletion} \\ \phi_F \ldots 2\phi_F & \text{in weak inversion} \\ 2\phi_F \ldots (2\phi_F + \Delta\phi) & \text{in moderate inversion} \\ > (2\phi_F + \Delta\phi) & \text{in strong inversion} \end{cases} \tag{3.52}$$

For simplicity, the front gate surface potential at threshold voltage is expected to be equal to $2\phi_F$ [Col04]. The threshold voltage V_{th} of SOI-MOSFETs is separately defined for partially depleted mode and fully depleted mode, which will be discussed in detail in the following sections.

3.6.1 Partially Depleted

In partially depleted mode, the threshold voltage of an N-channel SOI-MOSFET can be obtained from Equation (3.17), in case $\phi_{S1} = 2\phi_F$ and $Q'_d = -qN_{CH}x_{d1}$ [SN07]. Oxide charges are neglected in this analysis.

$$V_{th}|_{PD} = V_{FB1} + \phi_{S1} - \frac{Q'_d}{C'_{OX1}} = \phi_{ms1} + 2\phi_F + \frac{qN_{CH}x_{d1}}{C'_{OX1}} \tag{3.53}$$

As already discussed before, x_{d1} is strongly dependent on the surface potential ϕ_{S1}, temperature and doping concentration N_{CH}. When the device is partially depleted, Equation (3.53) can be rewritten with the expression of the depletion depth x_{d1} from (3.26) and results in

$$V_{th}|_{PD} = \phi_{ms1} + 2\phi_F + \frac{1}{C'_{OX1}}\sqrt{4\epsilon_{si}qN_{CH}\phi_F}\,. \tag{3.54}$$

It is worth mentioning here that the Fermi potential ϕ_F is a function of temperature and thereby it affects the threshold voltage over temperature, as can be seen from the derivation of the threshold voltage after temperature in Equation (3.55) [Col04].

$$\left.\frac{d}{dT}V_{th}\right|_{PD} = \frac{d\phi_{ms1}}{dT} + \frac{d\phi_F}{dT}\left(1 + \frac{q}{C'_{OX1}}\sqrt{\frac{\epsilon_{si}N_{CH}}{kTln\left(N_{CH}/n_i\right)}}\right) \tag{3.55}$$

3.6.2 Fully Depleted

In a fully depleted SOI-MOSFET device, the threshold voltage can be obtained from (3.30). Since the front gate surface potential ϕ_{S1} and the back gate surface potential ϕ_{S2} are coupled, the threshold voltage is strongly dependent on the back gate voltage V_{G2}. This dependency describes the so-called *back gate effect*. In this work, two back gate conditions are of great interest, i.e. the accumulated back interface and the depleted back interface. If the front interface is at threshold ($\phi_{S1} = 2\phi_F$), the back interface is accumulated ($\phi_{S2} = 0$) and the depletion charge is equal to $Q'_d = -qN_{CH}t_{SI}$, then the threshold voltage $V_{th}|_{acc}$ for an accumulated back interface is given by (3.56) [Col04].

$$V_{th}|_{acc} = \phi_{ms1} + 2\phi_F\left(1 + \frac{C_{si}}{C_{OX1}}\right) + \frac{qN_{CH}t_{SI}}{2C'_{OX1}} \tag{3.56}$$

The back gate voltage, at which the back interface becomes accumulated can be written as stated in Equation (3.57) [Col04].

$$V_{G2acc} = \phi_{ms2} - 2\phi_F\frac{C_{si}}{C_{OX2}} + \frac{qN_{CH}t_{SI}}{C'_{OX2}} \tag{3.57}$$

In case the back interface is depleted, the threshold voltage decreases with increasing back gate voltage and is given by [Col04]

$$V_{th}|_{depl} = V_{th}|_{acc} - \left(n|_{FD} - 1\right)\left(V_{G2} - V_{G2acc}\right)\ . \tag{3.58}$$

Since n is approximately 1.09 in fully depleted mode, as discussed in Section 3.2.2, the change in front gate threshold voltage caused by a change in back gate voltage is given by

$$\Delta V_{th}|_{depl} = -0.09\Delta V_{G2}\,. \tag{3.59}$$

The supply voltage of analog circuits considered in this work is 5 V, whereby the back gate voltage V_{G2} is at ground potential. The effective back gate bias

for P-channel SOI-MOSFETs is then equal to $-5\,\mathrm{V}$. With the estimation made in Equation (3.59), the threshold voltage of PMOS devices is decreased by approximately 450 mV. Compared to partially depleted SOI-MOSFET devices, there is no temperature dependence of the depletion charge in fully depleted SOI-MOSFETs [Col04]. As a result, the threshold voltage of fully depleted SOI-MOSFETs has a much lower temperature coefficient compared to partially depleted devices. The calculated, qualitative threshold voltage of an N-channel SOI-MOSFET with a channel doping concentration of $N_{CH} = 3 \cdot 10^{16}\,\mathrm{cm}^{-3}$ is shown in Figure 3.8.

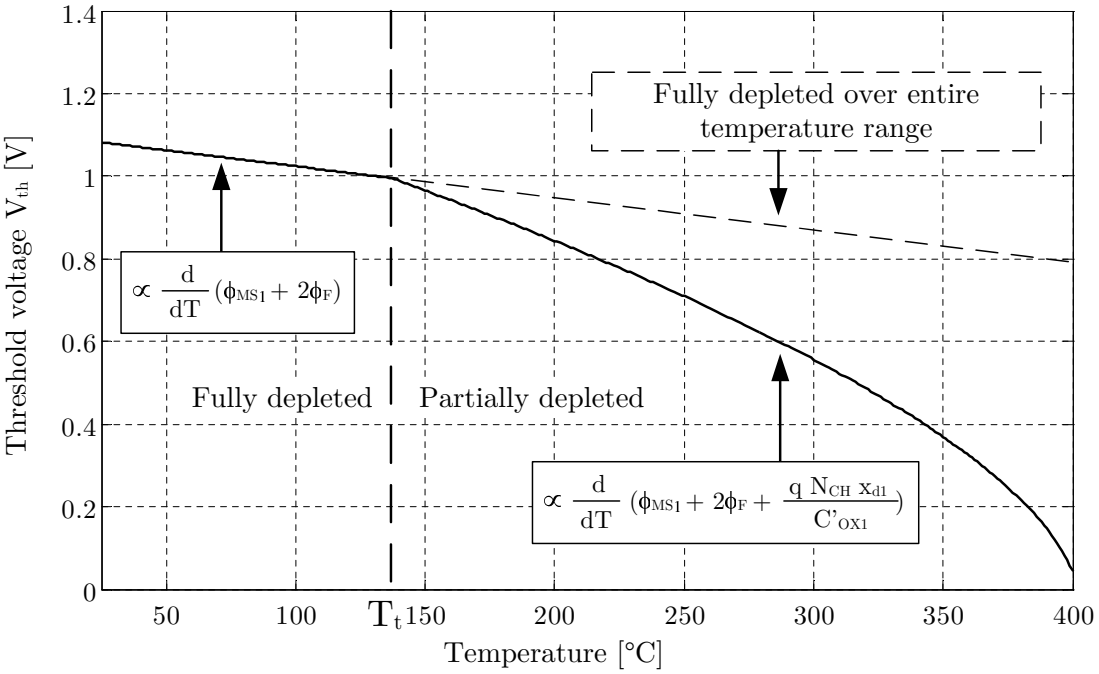

Figure 3.8: Qualitative threshold voltage over temperature, calculated using Equation (3.53). The transition temperature T_t from fully depleted to partially depleted is located at approximately 135 °C. The device is partially depleted at temperatures higher than the transition temperature.

The device is fully depleted up to a transition temperature of $T_t \approx 135\,^{\circ}\mathrm{C}$. The decrease of the threshold voltage with increasing temperature is linear and proportional to the flatband voltage $V_{FB} = \phi_{ms1}$ and the Fermi potential ϕ_F. Above the transition temperature, the threshold voltage decreases significantly with increasing temperature. The device is partially depleted in this temperature range. Thus, the depletion depth x_{d1} and the change in depletion charge Q'_d contribute to the change in threshold voltage. If the device would stay fully

depleted over the entire temperature range, the linear drop would persist up to 400 °C and more, as shown by the dashed line in Figure 3.8.

3.7 Body-Effect

The body-effect describes the modulation of the depletion region inside the silicon film of a partially depleted SOI-MOSFET caused by an applied body bias voltage V_B. In Figure 3.9, the film of the SOI-MOSFET is connected to the bias voltage V_B.

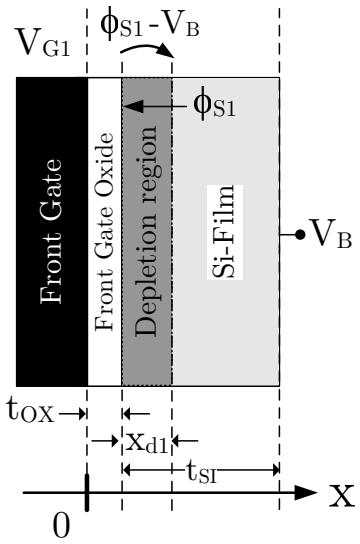

Figure 3.9: Metal-oxide-semiconductor structure at the front gate of an SOI-MOSFET with applied body bias voltage V_B. The effective voltage across the depletion region x_{d1} is equal to $\phi_{S1} - V_B$.

The voltage across the depletion region x_{d1} is then given by $\phi_{S1} - V_B$. Thus, the applied voltage V_B is equivalent to a decrease in surface potential ϕ_{S1} [YCF03] [SN07]. The depletion depth x_{d1} can then be rewritten as

$$x_{d1}\left(V_B\right) = \sqrt{\frac{2\epsilon_{si}\left(\phi_{S1} - V_B\right)}{qN_{CH}}} \,. \tag{3.60}$$

The change in depletion region depth directly affects the threshold voltage of partially depleted SOI-MOSFETs, since the number of ionized charges inside the depletion region is changed [Col98]. The expression of the threshold voltage, including the influence of the body bias V_B, can be adapted as written in Equation (3.61) [Col04].

$$V_{th}|_{PD}(V_B) = \phi_{ms1} + 2\phi_F + \frac{1}{C'_{OX1}}\sqrt{2\epsilon_{si}qN_{CH}(2\phi_F - V_B)}$$
$$= \phi_{ms1} + 2\phi_F + \gamma_1\sqrt{2\phi_F - V_B} \quad (3.61)$$

The body-effect coefficient was used to simplify the expression in Equation (3.61). The threshold voltage is decreased by an increase of body bias voltage V_B. On the other hand, the depletion depth x_{d1} is increased by a negative body-bias, which also increases the threshold voltage of partially depleted SOI-MOSFETs. It will be shown in Chapter 6 that the body-effect has a significant impact on the overall analog performance of SOI-MOSFETs and thereby also on the performance of analog circuits at high temperatures.

3.8 Leakage Currents

A current, which contributes to the drain current but cannot be controlled by the gate-source voltage, is usually defined as leakage current. Leakage currents can lead to malfunction of analog and digital circuits, as they dominate channel currents in SOI-MOSFETs at high temperatures. Various mechanisms inside the devices contribute to the leakage current level of SOI-MOSFETs. In this section, basic leakage mechanisms and their relevance for the investigation in this work are discussed.

Leakage currents of SOI-MOSFETs have been intensively studied [AB88] [LK99] [IRS+03]. Also the dependency of leakage currents on the channel length has been investigated [BAM01]. Three main leakage mechanisms contribute to the overall leakage current in the SOI-MOSFET, namely the PN-junction leakage current I_{PN}, the subthreshold leakage current I_{Sub} and the sidewall leakage current I_{SW}. Short channel effects (SCE) are neglected in this work, since long channel devices are usually preferred for analog circuit design. Figure 3.10 shows the qualitative channel current of an N-channel SOI-MOSFET at 25 °C and 200 °C.

In the 25 °C curve, the leakage current level at $V_{GS} = 0\,\text{V}$ is determined by the PN-junction leakage current. When the temperature increases, the transistor enters weak inversion, as it will be discussed later on. Therefore, the subthreshold leakage current increases with increased temperature and determines the leakage current level at $V_{GS} = 0\,\text{V}$. For the investigation of leakage currents in SOI-MOSFET devices in a wide temperature range, the temperature behavior of both leakage current mechanisms has to be analyzed, as shown in the following sections.

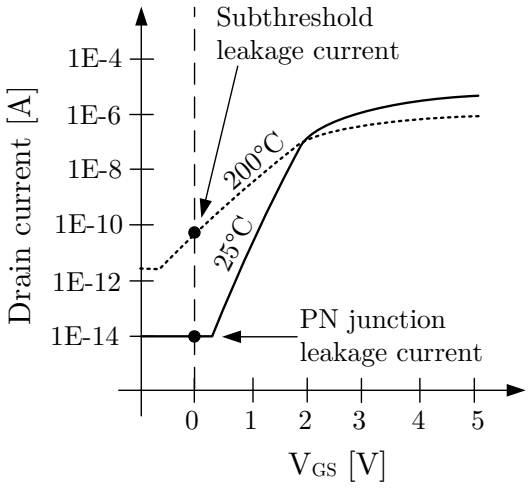

Figure 3.10: Qualitative channel current of an N-channel SOI-MOSFET and definition of leakage currents.

3.8.1 PN-Junction Leakage Current

The PN-junction leakage current I_{PN} is defined as the current, which is generated by the reverse bias of the drain-film or source-film PN-junctions. Figure 3.11 shows an N-channel SOI-MOSFET with the leakage current I_{PN}. The back gate depletion depth x_{d2} is neglected here for simplicity.

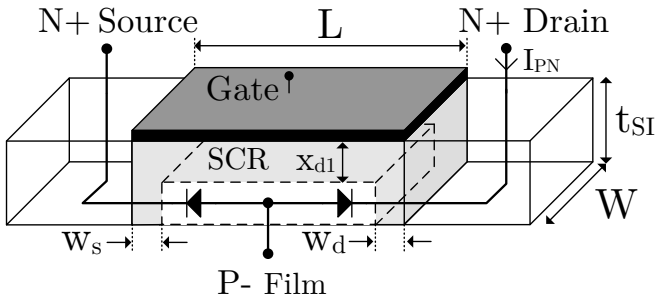

Figure 3.11: Illustration of the PN-junction leakage current I_{PN} through the reverse biased drain-film junction in a partially depleted N-channel SOI-MOSFET.

Two components contribute to the PN-leakage current, i.e. the diffusion current I_{DIFF} and the generation current I_G. Diffusion occurs on the edge of the neutral and the depleted regions inside the silicon film. Generation can occur inside the depleted film regions [SN07]. For the calculation of I_{PN}, the silicon film of the transistor is considered short-circuited with source. Also the depletion width w_d between the drain and the silicon film is neglected. The effective junction

area, where diffusion occurs is then given by $W \cdot L$, whereby the volume in which charge generation inside the depletion volume occurs, is given by $x_{d1} \cdot W \cdot L$.

For an N-channel SOI-MOSFET, the PN-junction leakage current, measured at the drain terminal, is the sum of both currents and can be written as [SN07]

$$I_{PN} = I_{DIFF} + I_G = W \cdot L \cdot q \sqrt{\frac{D_n}{\tau_n}} \frac{n_i^2}{N_{CH}} + \frac{x_{d1} \cdot W \cdot L \cdot q \cdot n_i}{\tau_g} \,. \tag{3.62}$$

In Equation (3.62), D_n is the diffusion constant of electrons, τ_n the lifetime of electrons in p-type silicon, W the device width, L the device length and τ_g the lifetime of generated charges in the depletion region [Col04][SN07][RLK+99]. In case of a fully depleted SOI-MOSFET, the depletion depth x_d extends to the maximum silicon film thickness t_{SI}. The generation current I_G thereby increases to I_{Gmax} and is given by

$$I_{Gmax} = \frac{t_{SI} \cdot W \cdot L \cdot q \cdot n_i}{\tau_g} \,. \tag{3.63}$$

Since diffusion occurs on the edge of the depletion region in SOI-MOSFET devices, the diffusion current I_{DIFF} can be neglected in FD state but should be considered in PD state [Col04][Wer96]. In partially depleted SOI-MOSFETs, the diffusion part becomes important mainly due to the charge reservoir in the neutral body region [ETVJR08]. A dominating influence of the generation current has also been reported for PD devices with high threshold voltage, which can occur in devices with a thin silicon film of around 40 nm [VKD+03]. Nevertheless, it will be shown in the next chapter that the diffusion mechanism also dominates the PN-junction leakage current at high temperatures in the considered SOI technology.

3.8.2 Subthreshold Leakage Current

In comparison to the PN-junction leakage current, the subthreshold leakage current has a strong dependency on the gate-source voltage. It is a consequence of the channel entering weak inversion with increasing gate-source voltage ($\phi_F < \phi_{S1} < 2\phi_F$). In Figure 3.10, on can see a linear dependency of the drain current on the gate-source voltage, for gate-source voltages higher than $V_{GS} = 0\,\mathrm{V}$ at 25 °C. Since Figure 3.10 is a semilogarithmic plot, the subthreshold current has an exponential dependency on the gate-source voltage. At high temperatures, the device enters weak inversion, even when the transistor is turned off by an applied gate-source voltage of $V_{GS} = 0\,\mathrm{V}$. Hence, weak inversion is primarily initiated by

temperature, rather than by gate-source voltage. To illustrate this relationship, the surface potential ϕ_{S1} and the Fermi potential ϕ_F are plotted over temperature in Figure 3.12.

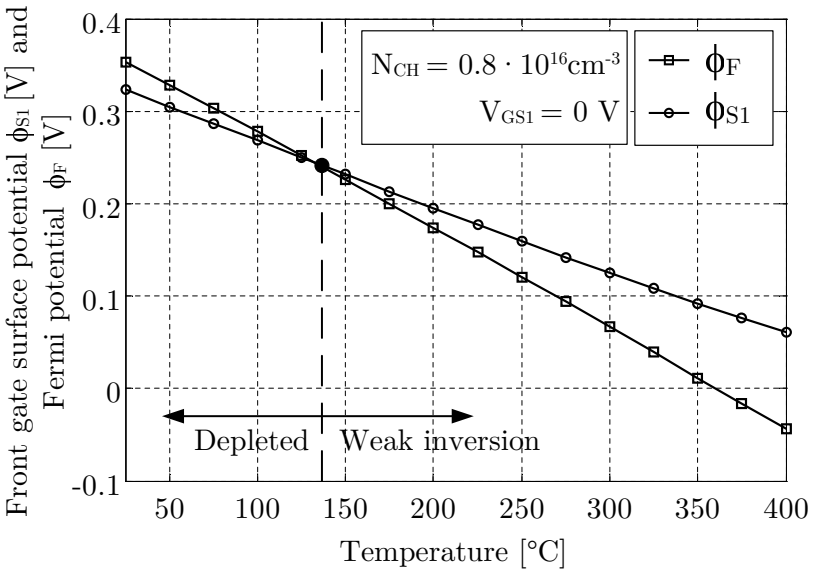

Figure 3.12: Front gate surface potential ϕ_{S1} and the Fermi potential ϕ_F over temperature for $V_{GS} = 0\,\mathrm{V}$ and a doping concentration of $0.8 \cdot 10^{16}\,\mathrm{cm}^{-3}$. The transition from depletion to inversion is located at approximately 135 °C.

The surface potential crosses the Fermi potential at approximately 135 °C. The channel is thereby in weak inversion for temperatures higher than that temperature. It has to be mentioned here that this transition point cannot easily be estimated analytically, due to a non-uniformly distributed channel doping concentration and an uncertainty in the calculation of the metal-semiconductor work function difference. Nevertheless, the calculated example illustrates the transition from depletion to weak inversion, which is caused by increased temperatures only. The subthreshold leakage current can be written as [RMMM03] [NR03]

$$I_{Sub} = \mu_0 C'_{OX1} \frac{W}{L} (n-1)\, V_t^2\, exp\left(\frac{V_{GS1} - V_{th}}{n \cdot V_t}\right)\left[1 - exp\left(\frac{-V_{DS}}{V_t}\right)\right] . \quad (3.64)$$

The last term in Equation (3.64) represents the dependency on the drain-source voltage V_{DS} and can be neglected for $V_{DS} \gg V_t$ [RMMM03]. The subthreshold leakage current depends mainly on the body factor n and the threshold voltage

V_{th}, and is thereby also strongly dependent on temperature, as it will be described in Chapter 4.

3.8.3 Sidewall Leakage Current

Within the considered SOI technology, a LOCOS (Local oxidation of silicon) process is used for the isolation of the transistor devices. The so called *bird's beak* at the edges of the SOI-MOSFET's channel causes a lower local doping concentration, which results in a decreased threshold voltage in that region. This effect can be modeled as an SOI-MOSFET device of the same type, but with decreased channel width and threshold voltage in parallel. The low threshold voltage of the parasitic device in parallel results in an additional leakage current I_{SW}. The qualitative channel current of an N-channel SOI-MOSFET with sidewall leakage current is shown in Figure 3.13.

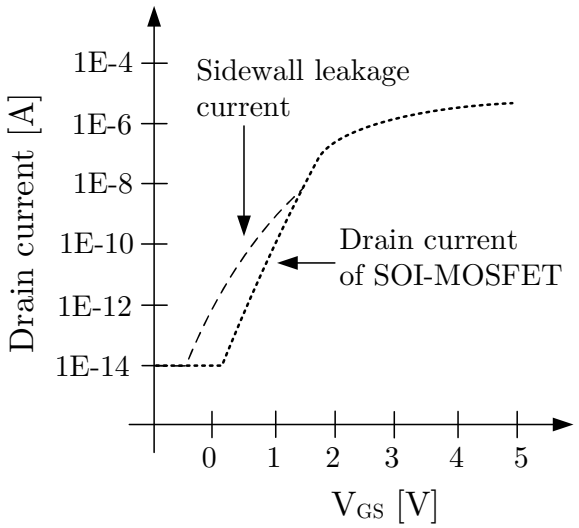

Figure 3.13: Qualitative sidewall leakage current in the weak inversion input characteristic of the SOI-MOSFET.

In the considered SOI technology, the appearance of sidewall leakage effect is suppressed by technology improvements. In Split-Source NSOI and PSOI devices, the sidewall leakage current is suppressed by silicon-sidewall body contacts (SSBC), located at each edge of the transistor's source region. The Split-Source NSOI transistor is depicted in Figure 3.14. In case an inversion layer exists inside the silicon film, the inverted N channel and the P^+ film contact form a reverse biased PN-junction. This PN-junction prevents a current flow from drain to source since the inverted sidewall channel is not connected to source.

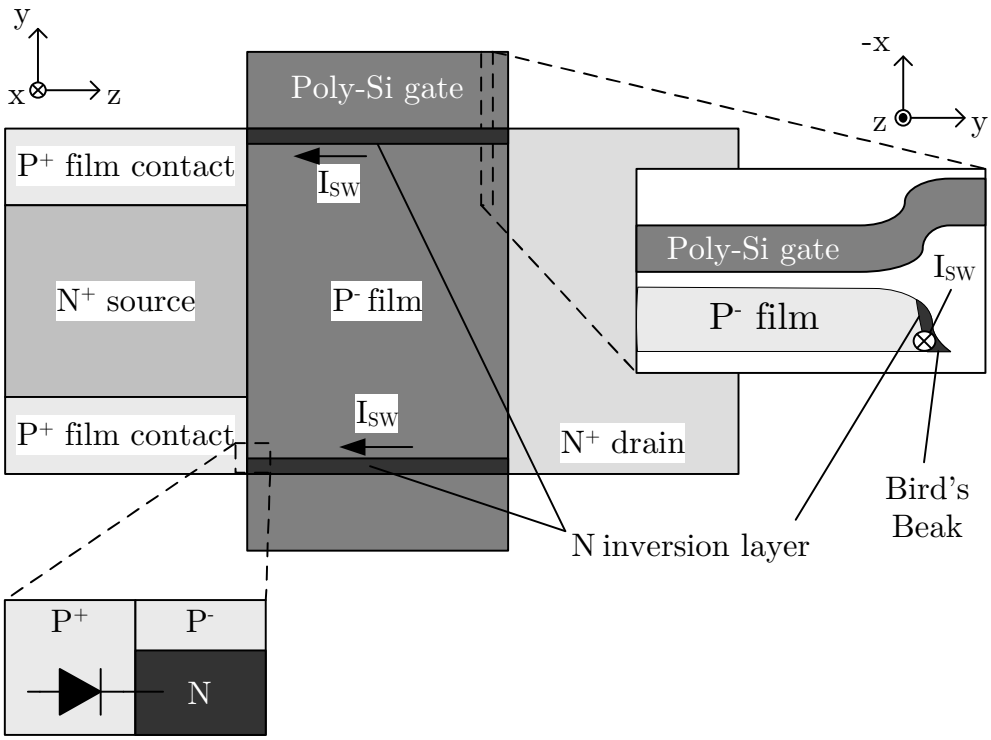

Figure 3.14: Top view of an NSOI-MOSFET with inversion layers on the edges of the silicon film.

The HGATE SOI-MOSFET effectively suppresses the sidewall leakage current due to its H-shaped gate. In consequence, the sidewall leakage current is effectively suppressed and is neglected in the further investigation of leakage mechanisms in SOI-MOSFET devices in the considered SOI technology.

3.9 Floating Body-Effects

Once the transistor is partially depleted, there is a neutral body region inside the silicon film, in which majority charge carriers can accumulate [Col04]. In an N-channel SOI device, the accumulation of holes in the silicon film is coupled with the increase of electrostatic potential in that region. A potential increase in the body region has a similar effect as the biasing of the film with a positive potential, which has been discussed before. Thereby, the threshold voltage is directly affected by floating body effects, i.e. it is decreased due to the accumulation of holes on the body region of N-channel SOI-MOSFETs and analogously by the accumulation of electrons in P-channel SOI-MOSFETs. Two floating body-effects are well known for abnormal current-voltage characteristics in SOI-MOSFETs, i.e. the

kink-effect and the *parasitic bipolar-effect*. Both effects and their relevance for the investigation in this work are discussed in the next sections.

3.9.1 Kink-Effect

The kink-effect is related to impact ionization in the high electric field region near the drain of SOI-MOSFETs [CF91]. Impact ionization is triggered at sufficiently high drain current and causes the generation of electron-hole pairs in the silicon film near the drain . Impact ionization decreases with increasing temperature [LK99]. Similar to the impact ionization current, the kink-effect can also be triggered by the PN-junction leakage current I_{PN}, which increases with temperature. The kink effect at high temperatures is therefore mainly caused by the reverse drain-film PN-junction leakage current. In an N-channel SOI-MOSFET, the generated electrons are drawn into the drain region or the inverted channel. The generated holes on the other hand, accumulate at the point of the lowest potential inside the non-depleted silicon film [Col04]. Figure 3.15 illustrates the currents, which contribute to the kink-effect in a partially depleted SOI-MOSFET.

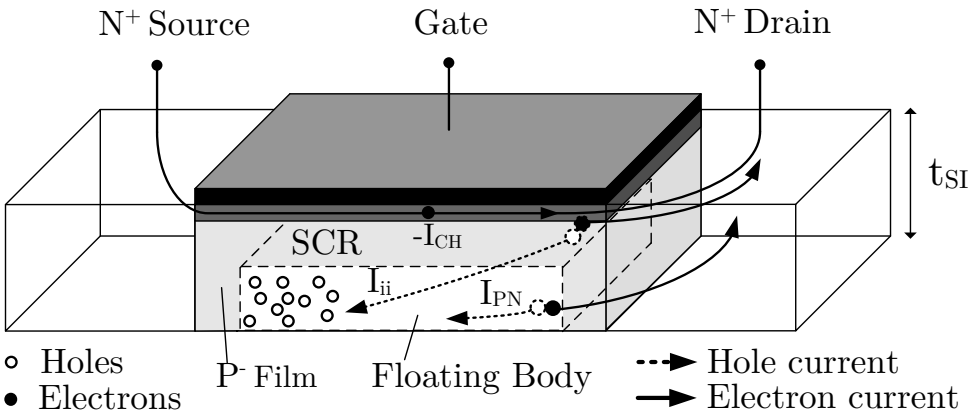

Figure 3.15: Inverted channel partially depleted SOI-MOSFET with floating body inside the silicon film region with impact ionization current I_{ii} and junction leakage current I_{PN}. Holes of both currents accumulate in the floating body region.

The accumulation of holes leads to decreased threshold voltage as the body potential increases. The drain current increases as a result of decreased threshold voltage. The increased drain current further increases the generation of electron-hole pairs in the silicon film. Although the kink-effect has also been reported for fully depleted transistors with large film-thicknesses [BMT+95], it is an effect

observed mainly in partially depleted SOI-MOSFETs [Col04]. The kink-effect can be reduced by a low resistive body-contact, which prevents accumulation of charges in the film region. In fully depleted SOI-MOSFETs, holes can more easily enter the source region, which is the result of the decreased PN-junction barrier, i.e. a built-in potential of $\Delta V_{bi} > 0$ [Col88] [CF91]. In case of potential barrier lowering, the kink-effect can be reduced significantly in FD SOI-MOSFETs [PW05].

3.9.2 Parasitic Bipolar-Effect

The parasitic bipolar effect describes the multiplication of the drain current in an SOI-MOSFET through a parasitic bipolar junction transistor (BJT). The parasitic bipolar transistor can be modeled as transistor in parallel to the regular SOI-MOSFET transistor as illustrated in Figure 3.16.

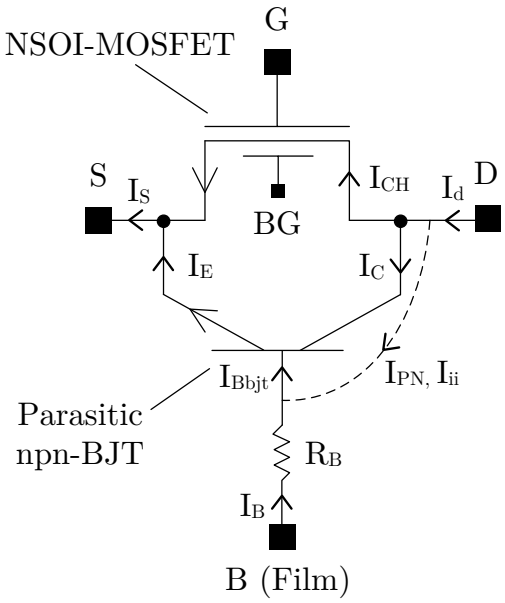

Figure 3.16: Parasitic npn bipolar junction transistor (npn-BJT) in parallel with the regular N-channel SOI-MOSFET and corresponding currents.

In Figure 3.16, BG is the back gate terminal, I_{CH} is the SOI-MOSFET channel current, I_E is the emitter current, I_C is the collector current, I_{Bbjt} is the base current, I_B is the body current, R_B is the body resistance, I_S is the source current and I_d is the drain current. The bipolar effect should be considered especially for partially depleted SOI-MOSFETs but has also been reported for fully depleted SOI-MOSFETs [CF91] [PNWP94] [SFCS+03]. It has been shown that an increased body resistance inside the silicon film can increase the parasitic bipolar current gain in SOI-MOSFETs [FMFC+00] [WOD10] [FCMG+02] [CSW+04]. In

a partially depleted SOI-MOSFET, the neutral body region acts as the base of the parasitic BJT, whereby the drain region is an equivalent to the collector and the source region represents the emitter. The relationship between collector current I_C, emitter current I_E and base current I_{Bbjt} is given by

$$I_C = \beta I_{Bbjt} \tag{3.65}$$

$$I_E = I_C + I_{Bbjt} \ . \tag{3.66}$$

In Equation (3.65), β is the common emitter current gain of the BJT given by [Col04]

$$\beta \approx 2\left(\frac{L_n}{L_B}\right)^2 - 1 \approx \frac{2D_n\tau_n}{L_B^2} - 1 \ , \tag{3.67}$$

where L_n is the diffusion length of electrons and L_B is the length of the base region. Using the Einstein relation, $D_n = V_t\mu_n$, Equation (3.67) can be rewritten as [Col04]

$$\beta \approx 2V_t\frac{\mu_n\tau_n}{L_B^2} - 1 \ . \tag{3.68}$$

One can see that β is inversely proportional to the square of the channel length. Thereby, β decreases rapidly with increasing channel length and is considered small for long channel SOI-MOSFETs. Nevertheless, the bipolar effect can lead to an increase of the overall drain current of the SOI-MOSFET device as leakage currents at high temperatures act as base current for the parasitic bipolar device [PNWP94] [FMFC+00].

3.10 The g_m/I_d Figure of Merit

Analog circuits have to fulfill various specifications, e.g. high accuracy and operating speeds. At the same time, these circuits must not consume much power in low power applications, e.g. for RFID (Radio Frequency Identification) applications. In case the primary constraint is power consumption, a specific quiescent- and operating current is allowed for every building block within a more complex analog circuit. The g_m/I_d design method can be used to determine the device dimensions according to given gain and bandwidth requirements, once a maximum operating current has been specified. The g_m/I_d factor, also called the transconductance efficiency, is a central figure of merit for analog circuit design.

The corresponding design approach with respect to high temperature operation is discussed in the following sections.

The derivation of the g_m/I_d factor is based on the work of Enz, Krummenacher and Vitoz [EKV95] and was developed further in [ECF+96] [FECJ94] [FBB02] [BHT+03] [CC04] [Bin07a] [HCC05]. Also the advantage of fully depleted SOI-MOSFETs over partially depleted SOI-MOSFETs and bulk devices was demonstrated in these works. Since the focus of this work is on analog circuit design at high temperatures, essential analog parameters like intrinsic gain and bandwidth are described in the following sections and evaluated over temperature in Chapter 4.

3.10.1 g_m/I_d Factor in all Regions of Operation

The drain current of an SOI-MOSFET in weak inversion for a drain voltage of $V_{DS} \gg V_t$ can be expressed as [EKV95] [Bin07b]

$$I_d|_{WI} = 2n\mu_0 C'_{OX1}\frac{W}{L}V_t^2\, exp\left(\frac{V_{GS1} - V_{th}}{n \cdot V_t}\right) . \tag{3.69}$$

The small signal transconductance $g_m|_{WI}$ in weak inversion can be obtained by differentiating Equation (3.69) once with respect to V_{GS1} and is given by

$$g_m|_{WI} = \frac{\partial I_d}{\partial V_{GS1}} = \frac{I_d}{nV_t} . \tag{3.70}$$

If Equation (3.70) is divided by I_d, one obtains the expression for the transconductance efficiency in weak inversion, which is given by

$$\left.\frac{g_m}{I_d}\right|_{WI} = \frac{1}{nV_t} . \tag{3.71}$$

The value of the transconductance efficiency in weak inversion is mainly determined by n. Since n is approximately 1.09 for FD-SOI-MOSFETs, the g_m/I_d factor at room temperature (25 °C) is 35.7 V^{-1}, with a thermal voltage of $V_t = 25.7$ mV. This value is close to its theoretical maximum of 38.9 V^{-1} ($n = 1$). Neglecting the channel length modulation (CLM), the drain current $I_d|_{SI}$ in strong inversion is given by (3.72) [Bin07b].

$$I_d|_{SI} = \frac{\mu_0 C'_{OX1} W}{2nL}(V_{GS1} - V_{th})^2 \tag{3.72}$$

The transconductance in strong inversion can also be obtained from the derivation of Equation (3.72) after V_{GS1}

$$g_m|_{SI} = \frac{\partial I_d}{\partial V_{GS1}} = \frac{\mu_0 C'_{OX1} W}{nL} (V_{GS1} - V_{th}) = \frac{2I_d}{V_{GS1} - V_{th}} . \tag{3.73}$$

The transconductance efficiency of an SOI-MOSFET in strong inversion can then be written as [Bin07b]

$$\left.\frac{g_m}{I_d}\right|_{SI} = \frac{2}{V_{GS1} - V_{th}} = 2 \left(\sqrt{\frac{2nI_d L}{\mu_0 C'_{OX1} W}} \right)^{-1} = \sqrt{\frac{2\mu_0 C'_{OX1} W}{nI_d L}} . \tag{3.74}$$

It is worth mentioning here that the transconductance efficiency g_m/I_d in weak inversion is not a function of drain current I_d, whereby it is inversely proportional to the square-root of the drain current in strong inversion.

$$\left.\frac{g_m}{I_d}\right|_{WI} \neq f(I_d) \tag{3.75}$$

$$\left.\frac{g_m}{I_d}\right|_{SI} \propto \frac{1}{\sqrt{I_d}} \tag{3.76}$$

The transconductance efficiency for all regions of operation has been discussed in the work of [EKV95] and also is described in [Bin07b]. In order to obtain the drain current in moderate inversion, the weak inversion expression in Equation (3.71) and the strong inversion expression in Equation (3.74) can be used. The drain current in moderate inversion is then obtained by setting both equations equal and solving the resulting expression for $I_d|_{MI}$.

$$\frac{1}{nV_t} = \sqrt{\frac{2\mu_0 C'_{OX1} W}{n\, I_d|_{MI}\, L}} \rightarrow I_d|_{MI} = 2\mu_0 C'_{OX1} n V_t^2 \left(\frac{W}{L}\right) \tag{3.77}$$

The normalized drain current in moderate inversion $I_d|_{MI}/(W/L)$ is independent of the device geometry and thereby characteristic for every type of transistor within a specific technology [Bin07b]. It is often referred to as the *technology current* I_0 or *specific current* i_f [EKV95]. It is given by [Bin07b]

$$I_0 = \frac{I_d|_{MI}}{\left(\frac{W}{L}\right)} = 2\mu_0 C'_{OX1} n V_t^2 . \tag{3.78}$$

The technology current I_0 is expected to exhibit some change with varying temperature, since it is a function of the zero-field charge carrier mobility μ_0, the body factor n, and the thermal voltage V_t. The temperature dependence of the technology current I_0 will be discussed in detail in the next section.

The derivations made in [EKV95] and [Bin07b] were used in order to obtain an expression for the transconductance efficiency from weak inversion to strong inversion. It can be written as [EKV95]

$$\left.\frac{g_m}{I_d}\right|_{WI\to SI} = \frac{1}{nV_t\sqrt{IC+0.5\sqrt{IC}+1}}\,. \tag{3.79}$$

where IC is the inversion coefficient, which will be discussed in Section 3.10.3. The expression in Equation (3.79) can be simplified further without loosing significant accuracy and is given by [EKV95]

$$\left.\frac{g_m}{I_d}\right|_{WI\to SI} = \frac{1}{nV_t\left(\sqrt{IC+0.25}+0.5\right)}\,. \tag{3.80}$$

Equation (3.80) is valid in all regions of operation, i.e. from weak inversion to strong inversion [Bin07b] and is used to illustrate the distribution of g_m/I_d over drain current I_d and for different temperatures in Figure 3.17.

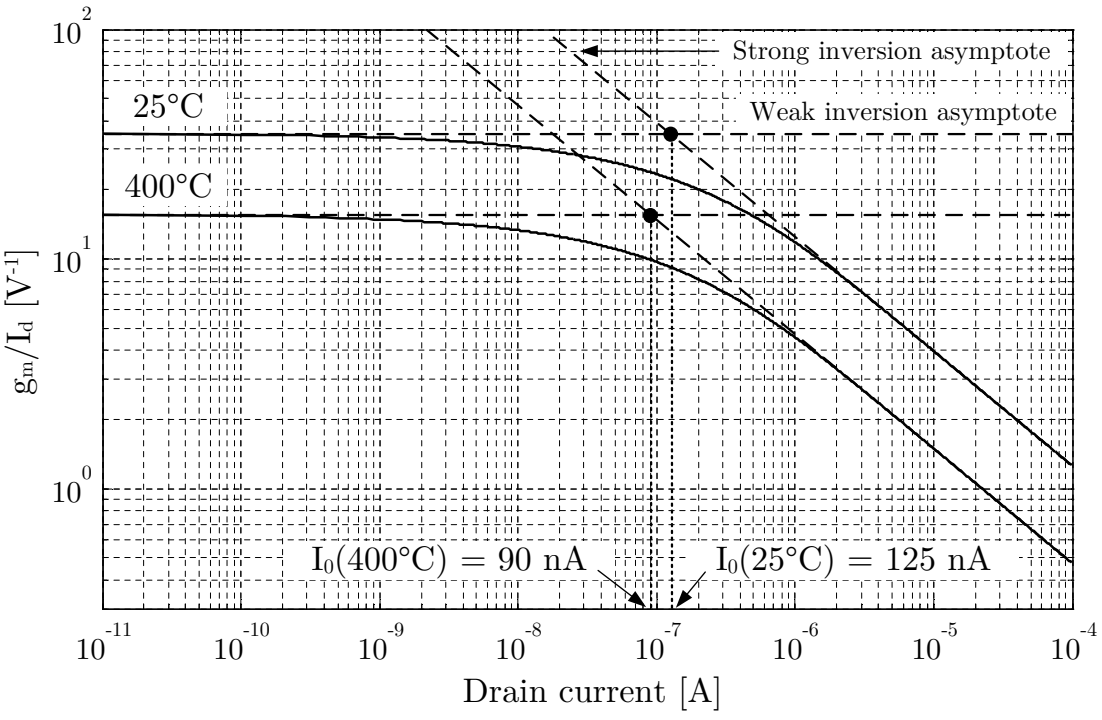

Figure 3.17: Transconductance efficiency g_m/I_d over drain current I_d for different temperatures. The technology current I_0 can be obtained from the intersection of the tangents in weak inversion and strong inversion.

One can see that the transconductance efficiency in the weak inversion region is independent of drain current. In strong inversion, it decreases due to the inverse

proportional relationship to the drain current $\left(g_m/I_d \propto 1/\sqrt{I_d}\right)$. The technology current I_0 can be obtained graphically by the intersection of the weak inversion and strong inversion asymptote, equivalent to the calculation of the technology current in (3.77). At a temperature of 25 °C, the technology current is $I_0 = 125\,\text{nA}$. For increasing temperatures, the overall g_m/I_d value decreases due to the influence of the thermal voltage V_t. In this example, the technology current decreases with increasing temperature, which is due to a strong influence of the zero-field charge carrier mobility μ_0. Nevertheless, I_0 may also increase with increasing temperature in case the temperature exponent of the charge carrier mobility μ_0 in the specific technology is smaller.

3.10.2 Technology Current

The technology current is defined as the normalized drain current in the center of the moderate inversion region of SOI-MOSFETs and is independent of device geometry [Bin07b]. It is once again written in Equation (3.81) in order to emphasize it's temperature dependence.

$$I_0\left(T\right) = 2\mu_0\left(T\right) C'_{OX1} n\left(T\right) V_t^2\left(T\right) \tag{3.81}$$

In the work of [Bin07b], a fixed technology current has been used to simplify hand calculations. The fixed technology current is independent on temperature variations of the body coefficient n and charge carrier mobility μ_0. It was shown in [Bin07b] that the accuracy of this simplification is sufficient for the military temperature range, i.e. up to 125 °C [Bin07b]. However, in this work, the considered temperature range is significantly higher and reaches up to 400 °C. A more detailed temperature analysis of the technology current will be discussed in Section 4.4.2.

3.10.3 Inversion Coefficient

The inversion coefficient IC can be used as a numeric indicator for the MOSFET's state of inversion. The use of the inversion coefficient simplifies hand calculations when corresponding device geometries for a specific drain current have to be found. The inversion coefficient is defined as the drain current divided by the technology current and the W/L ratio and is written in Equation (3.82) [Bin07b][BHT+03].

$$IC = \frac{I_d}{I_0\left(\frac{W}{L}\right)} = \frac{I_d}{2\mu_0 C'_{OX1} n V_t^2\left(\frac{W}{L}\right)} \tag{3.82}$$

An inversion coefficient of 1 corresponds to the center of moderate inversion [Bin07b]. Figure 3.18 depicts the inversion coefficient of the MOSFET in all regions of operation (adapted from [Bin07b]).

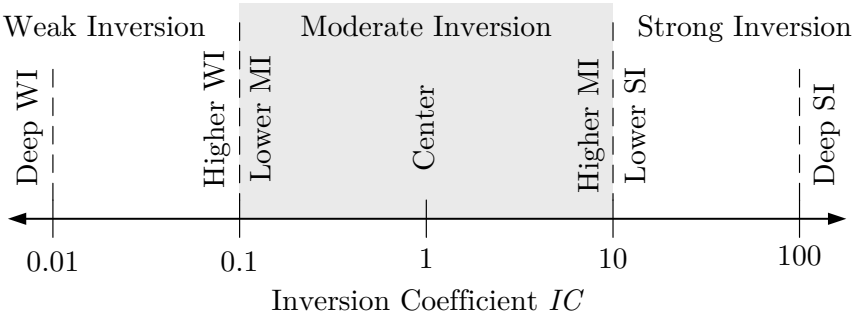

Figure 3.18: Inversion coefficient in all regions of operation, i.e. from weak inversion to strong inversion (adapted from [Bin07b]).

It can be seen from Figure 3.18 that an inversion coefficient in the range of $0.1 \ldots 10$ corresponds to the moderate inversion region. As the technology current varies with temperature, as discussed in the previous section, also the inversion coefficient changes with temperature and constant drain current. The variation of I_0 and thereby IC with temperature, can be neglected for fully depleted SOI-MOSFETs, but is relevant for partially depleted SOI-MOSFETs and will be discussed in more detail in Section 4.4.2.

3.11 Intrinsic Gain and Intrinsic Bandwidth

The gate-to-drain voltage gain of a common source gain stage is referred to as intrinsic gain of the MOSFET device [Bin07b]. The source of the intrinsic gain stage is grounded and the drain is connected to an ideal current source. Intrinsic gain is the maximum achievable gain of a single transistor device [Bin07a]. Figure 3.19 illustrates an intrinsic gain stage with an N-channel SOI-MOSFET M_1 and a load capacitance C_L. The equivalent small signal circuit for low frequencies of the SOI-MOSFET M_1 is shown in Figure 3.20.

In Figure 3.20, r_{ds} is the drain-source small signal resistance, C_{GSi} the intrinsic gate-source capacitance, C_{GDi} the intrinsic gate-drain capacitance, C_{GBi} the intrinsic gate-film capacitance, C_{DBi} the intrinsic drain-film capacitance and C_{SBi} the intrinsic source-film capacitance. In case of the intrinsic gain stage, the film terminal (B) is short-circuited with the source terminal (S). Intrinsic capacitances can be neglected for the calculation of the open loop DC gain of the SOI-MOSFET.

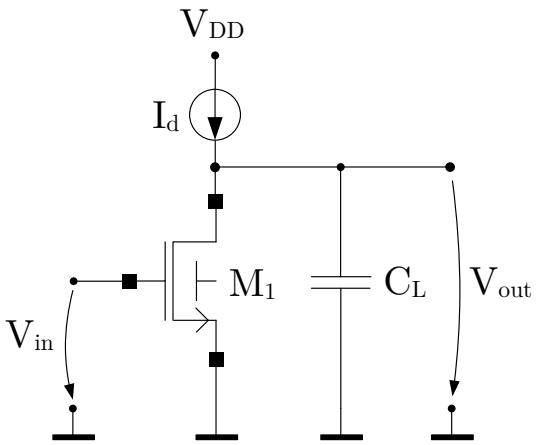

Figure 3.19: Intrinsic gain stage with an N-channel SOI-MOSFET M_1 and load capacitance C_L.

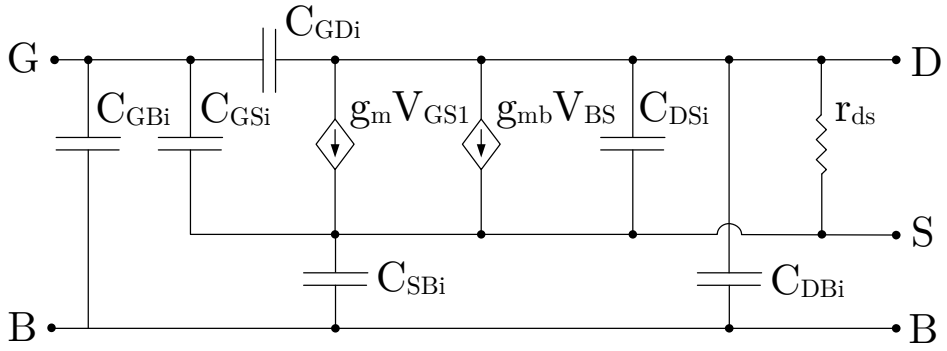

Figure 3.20: Small signal equivalent circuit of an SOI-MOSFET for low frequencies.

The open loop DC gain of the intrinsic gain stage can be calculated using the transconductance g_m and the drain-source resistance r_{ds}, or the transconductance efficiency g_m/I_d and the Early voltage V_A and is given by (3.83) [Bin07b].

$$A_i = \frac{v_{out}}{v_{in}} = -g_m \cdot r_{ds} = -\frac{g_m}{g_{ds}} = -\left(\frac{g_m}{I_d}\right) V_A \tag{3.83}$$

In Equation (3.83), g_{ds} is the drain-source small-signal conductance and V_A is the Early voltage, which is given by

$$V_A = \frac{I_d}{g_{ds}} \,. \tag{3.84}$$

Using the expression for the transconductance efficiency in all regions of operation from Equation (3.80), the intrinsic gain can be rewritten as given in (3.85) [Bin07b] [BHT+03].

$$A_i = -\frac{V_A}{nV_t\left(\sqrt{IC+0.25}+0.5\right)} \tag{3.85}$$

The intrinsic bandwidth, i.e. the transition frequency where the gain of the intrinsic gain stage is one, can be calculated using Equation (3.86) [Bin07b].

$$f_T = \frac{g_m}{2\pi\left(C_{GSi}+C_{GBi}\right)} \tag{3.86}$$

The intrinsic bandwidth can be expressed in terms of the inversion coefficient IC and channel length L. It is then given by [Bin07b]

$$f_T = \left(\frac{IC}{\left(\sqrt{IC+0.25}+0.5\right)}\right)\left(\frac{\mu_0 V_t}{\pi\left(\hat{C}_{GSi}+\hat{C}_{GBi}\right)L^2}\right) . \tag{3.87}$$

In Equation (3.87), $\hat{C}_{GSi}$ is the intrinsic gate-source capacitance and $\hat{C}_{GBi}$ the intrinsic gate-body capacitance, both normalized to the gate-oxide capacitance. The sum of both capacitances in all regions of operation is given by [Bin07b]

$$\left(\hat{C}_{GSi}+\hat{C}_{GBi}\right) = \begin{cases} \frac{n-1}{n} & \text{in weak inversion} \\ \frac{n-2/3}{n} & \text{in moderate inversion} \\ \frac{n-1/3}{n} & \text{in strong inversion} \end{cases} . \tag{3.88}$$

Expression (3.87) will be used later on in Chapter 4 for the discussion on intrinsic bandwidth of partially depleted and fully depleted SOI-MOSFETs at high temperatures.

3.12 Early Voltage

The drain-source conductance describes the increase in drain current I_d caused by an increase in drain-source voltage V_{DS}. For small-signal operation, the small-signal drain-source conductance g_{ds} is the partial derivative of the drain current I_d after the drain-source voltage V_{DS} and is given by Equation (3.89) [Bin07b].

$$g_{ds} = \frac{\partial I_d}{\partial V_{DS}} = \frac{1}{r_{ds}} \tag{3.89}$$

In (3.89), r_{ds} is the drain-source resistance. The increase in drain current is caused by the modulation of effective channel length, also referred to as channel length modulation (CLM). The resulting drain current I_d can be described by the sum of the drain current without channel length modulation and the drain current resulting from channel length modulation [Bin07b].

$$I_d = I_d\,(\text{without CLM}) + I_d\,(\text{CLM}) = I_d\,(\text{without CLM})\,(1 + \lambda V_{DS}) \tag{3.90}$$

In (3.90), λ is the channel length modulation factor, which is given by [Bin07b]

$$\lambda = \frac{1}{V_A}\,. \tag{3.91}$$

Since the Early voltage is determined by the intersection of the tangent in the SOI-MOSFET's output characteristic with the V_{DS} axis, it is specified in negative voltage values. Nevertheless, in this work absolute values of the Early voltage are used. The Early voltage is a function of drain-source voltage V_{DS} and channel length L.

$$V_A = f\,(V_{DS}, L) \tag{3.92}$$

In this work, the dependency of the Early voltage on the drain-source voltage V_{DS} is included in the expression of the Early voltage. This consideration is useful when the Early voltage is investigated as a function of drain current for a given drain-source voltage in the following chapters. Thus, the drain-source voltage is always specified for a given Early voltage.

As already mentioned, the Early voltage is also depended on channel length. With increased channel length, the drain-source voltage V_{DS} has a decreased effect on the overall channel current. Thereby, the Early voltage is higher for long channel devices. Drain induced barrier lowering (DIBL) is also negligible for long channel devices and does not affect the Early voltage in this case [Bin07b]. As a consequence, long channel SOI-MOSFET devices offer a much higher intrinsic gain than short channel devices and are therefore preferred for analog circuit design.

3.13 Summary

Within this chapter, fundamental SOI-MOSFET device characteristics were discussed in order to prepare the investigation and the discussion in the following chapters. As a major cause of high temperature device performance degradation, the change of depletion state with increasing temperature was theoretically analyzed. The resulting analog parameters, e.g. threshold voltage, subthreshold voltage swing and also leakage currents in partially depleted and fully depleted SOI-MOSFETs were presented and discussed. As major performance parameters, the g_m/I_d factor, Early voltage and intrinsic gain and bandwidth were introduced.

In the following chapter, the temperature dependencies of these fundamental SOI-MOSFET device characteristics are discussed as a function of temperature and are evaluated by experimental results up to 400 °C in the considered SOI technology.

Chapter 4

SOI-MOSFET Characteristics in a Wide Temperature Range

In order to prepare the discussions in the following chapter, the considered SOI technology, as well as fundamental SOI-MOSFET device physics were described in the previous chapter. The theoretical upper temperature limit of SOI technology depends on the doping concentration of the silicon film. Different values can therefore be found in literature. The temperature limitations of analog circuits fabricated in SOI technology are discussed in this section. First focusing on the maximum operating temperature of circuits in the considered SOI technology, fundamental SOI-MOSFET device characteristics, e.g. threshold voltage and leakage currents at high temperatures are further investigated in the next step.

4.1 Limitations of SOI Technology

The intrinsic carrier concentration as a function of temperature T, expressed in Kelvin is given by (4.1) [Col04].

$$n_i = 3.9 \cdot 10^{16} \cdot T^{3/2} \cdot exp\left(\frac{-E_G(0)}{2kT}\right) \tag{4.1}$$

The majority carrier concentration n_0 in n-type semiconductors ($N_D \gg N_A$) can be obtained from combining the law of mass actions in semiconductors at thermal equilibrium given in (4.2) [SN07]

$$n_0 \cdot p_0 = n_i^2 \tag{4.2}$$

with the charge neutrality condition at thermal equilibrium given by Equation (4.3) [SN07].

$$n_0 + N_A = p_0 + N_D \ . \tag{4.3}$$

Solving Equation (4.3) for n_0 with $N_A = 0$ yields the majority carrier concentration [SN07].

$$n_0 \approx \frac{1}{2}\left[\sqrt{N_D^2 + 4n_i^2} + N_D\right] \tag{4.4}$$

The intrinsic carrier concentration n_i, as well as the majority carrier concentration $n_0\,(N_{Di})$ in an n-type semiconductor over temperature and three different doping concentrations N_{Di} are shown in Figure 4.1.

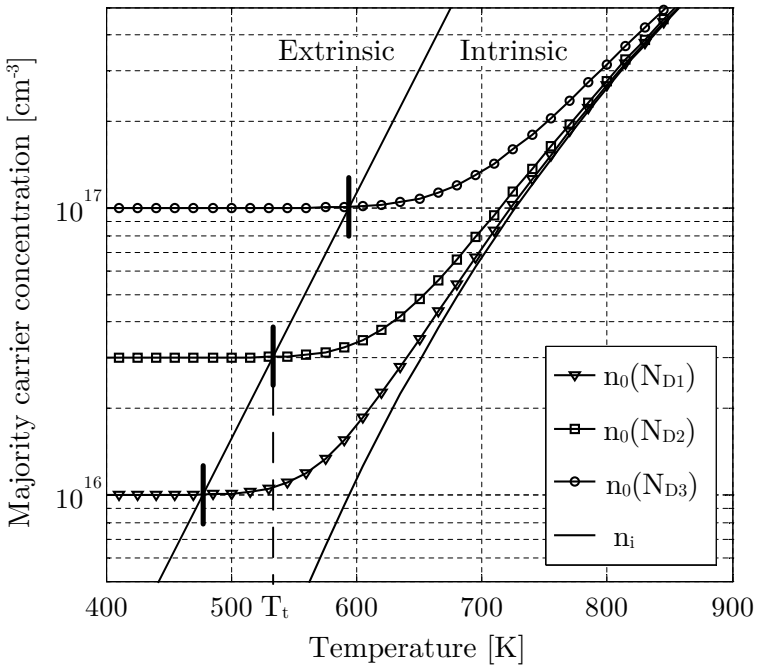

Figure 4.1: Intrinsic carrier concentration n_i and majority carrier concentration $n_0\,(N_{Di})$ for different doping concentrations N_{Di} in n-type silicon over temperature.

Below a transition temperature T_t, the amount of majority charge carriers $n_0\,(N_{Di})$ is mainly determined by the doping concentration N_{Di}. Above the transition temperature T_t, the silicon semiconductor turns from extrinsic to intrinsic and $n_0\,(N_{Di})$ becomes a strong function of temperature. For a doping concentration of $N_{D2} = 3 \cdot 10^{16}\,\mathrm{cm}^{-3}$, the transition temperature T_t is approximately 530 K, which is equal to 257 °C.

It can also be seen from Figure 4.1 that the transition temperature T_t moves to higher temperatures with increasing doping concentration. Although the operation of silicon in the intrinsic temperature range is feasible, device leakage currents

are significantly increased by the increase of the majority carrier concentration. As a matter of fact, leakage currents increase rapidly, once the silicon becomes intrinsic. In analog and digital circuits, increased leakage currents are responsible for reduced accuracy, decreased circuit performance or even malfunctions. It is therefore necessary to reduce the leakage current level in order to operate these circuits at elevated temperatures up to 400 °C.

4.2 Threshold Voltage at High Temperatures

The threshold voltage of partially depleted and fully depleted SOI-MOSFETs decrease with increasing temperature. Responsible for the decrease is the change in flatband voltage V_{FB} and the change in depletion charge beneath the gate of the device. Due to the resulting self-conductance of SOI-MOSFET devices at high temperatures, the decrease in threshold voltage can be critical for circuit operation. Even if the transistor is turned off by a gate-source voltage of $V_{GS} = 0\,\mathrm{V}$, the drain current can be dominated by leakage currents at high temperatures. These leakage currents lead to an increased static quiescent current in analog and digital circuits at high temperatures. The main leakage current contributor is the subthreshold leakage current I_{Sub}, which is dependent on the threshold voltage. Therefore, a sufficient high threshold voltage has to be guaranteed, especially at high temperatures.

The threshold voltages of Split-Source NSOI and NHGATE devices were experimentally obtained for temperatures up to 400 °C. The measurements were carried out in an high temperature oven. The entire measurement setup is described in details in appendix A.2. The threshold voltage was extracted from the input characteristic curve I_d over V_{GS}, using the tangent method at the point of maximum slope (g_{mMAX}). The results were evaluated using MATLAB[1]. The evaluation procedure as well as the corresponding MATLAB script are presented in appendix B. The measured threshold voltage over temperature is shown in Figure 4.2. The film contact of the HGATE transistor is short-circuited with source ($V_{BS} = 0V$). The back gate-source voltage of both devices is zero ($V_{BGS} = 0\,\mathrm{V}$).

It can be seen from Figure 4.2 that the temperature dependence of both threshold voltages is similar. Both threshold voltages decrease non-linearly with increasing temperature. This non-linear decrease indicates that the devices become partially depleted at higher temperatures. At a temperature of 400 °C, the remaining threshold voltages of both devices is less than 200 mV. It can

[1] MATLAB is a registered trademark of The MathWorks, Inc.

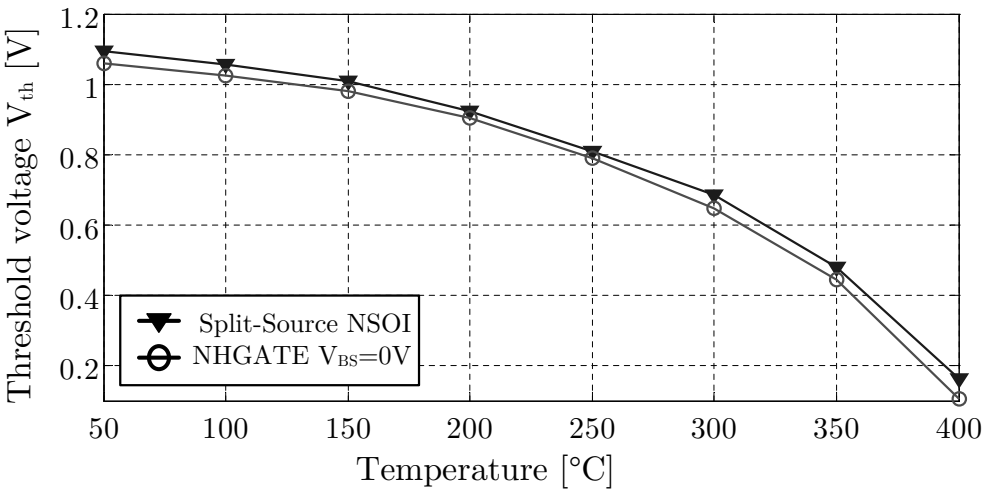

Figure 4.2: Measured threshold voltages of Split-Source NSOI-MOSFETs and NHGATE SOI-MOSFETs over temperature with $V_{BGS} = 0V$.

be expected from these measurements that the subthreshold leakage current is significantly increased by the low threshold voltage, as we will see in the following section.

Experimentally obtained threshold voltages of N-channel and P-channel Split-Source SOI-MOSFETs over temperature are shown in Figure 4.3. The threshold voltages are shown in solid lines. For better comparison between linear and non-linear degradation, the linear degradation in fully depleted mode was extrapolated to higher temperatures and is shown by dashed lines. The threshold voltage of NSOI-MOSFETs decreases linearly up to a temperature of approximately 125 °C. At higher temperatures, a non-linear decrease can be recognized, which is related to the transition from fully depleted to partially depleted at high temperatures. The temperature, at which the transition is located, is in good agreement with the theoretical expectations developed earlier in Section 3.6.

The threshold voltage of Split-Source SOI-MOSFETs was measured without back gate effect ($V_{BGS} = 0\,\mathrm{V}$). The resulting overall absolute threshold voltage of Split-Source P-channel SOI-MOSFETs is higher compared to N-channel devices. A transition from fully depleted to partially depleted can also be recognized for P-channel devices. The transition temperature is located at approximately 200 °C. It is higher than for N-channel devices due to a lower channel doping concentration for P-channel SOI-MOSFETs and a higher back gate depletion depth x_{d2} at the back interface, i.e. the back gate effect. The remaining threshold voltage at 400 °C is approximately $-0.5\,\mathrm{V}$ and thereby higher than the threshold voltage of N-channel devices. When the back gate effect is considered for PMOS devices,

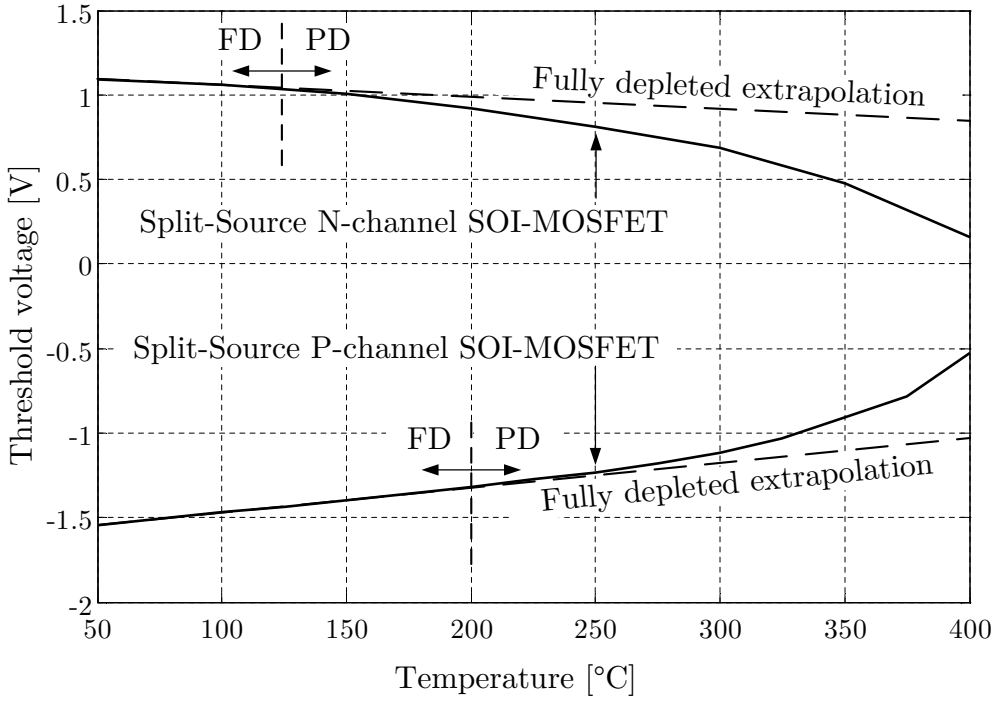

Figure 4.3: Measured threshold voltage of N-channel and P-channel Split-Source SOI-MOSFETs over temperature. The back gate source voltages and body-source voltages of both devices are $V_{BGS} = 0\,\mathrm{V}$ and $V_{BS} = 0\,\mathrm{V}$, respectively.

the threshold voltage of both devices at 400 °C is too low to prevent severe leakage currents. Relevant leakage current mechanisms and their dependencies on temperature are explained in the following section.

4.3 Leakage Currents

The cause of leakage currents in SOI-MOSFETs was discussed in Section 3.8. In case sidewall leakage currents are neglected, the main contributors to the overall leakage current are the PN-junction leakage current and the subthreshold leakage current. Since both, the subthreshold leakage current and the PN-junction leakage current are proportional to the device width W, leakage currents are especially critical for devices with large channel widths. In order to determine the leakage current mechanisms in the considered SOI technology, leakage currents were experimentally investigated for temperature up to 400 °C. Figure 4.4 shows the weak inversion input characteristics of an N-channel SOI-MOSFET as a function of gate-source voltage V_{GS} for different temperatures from 50 °C up to 400 °C.

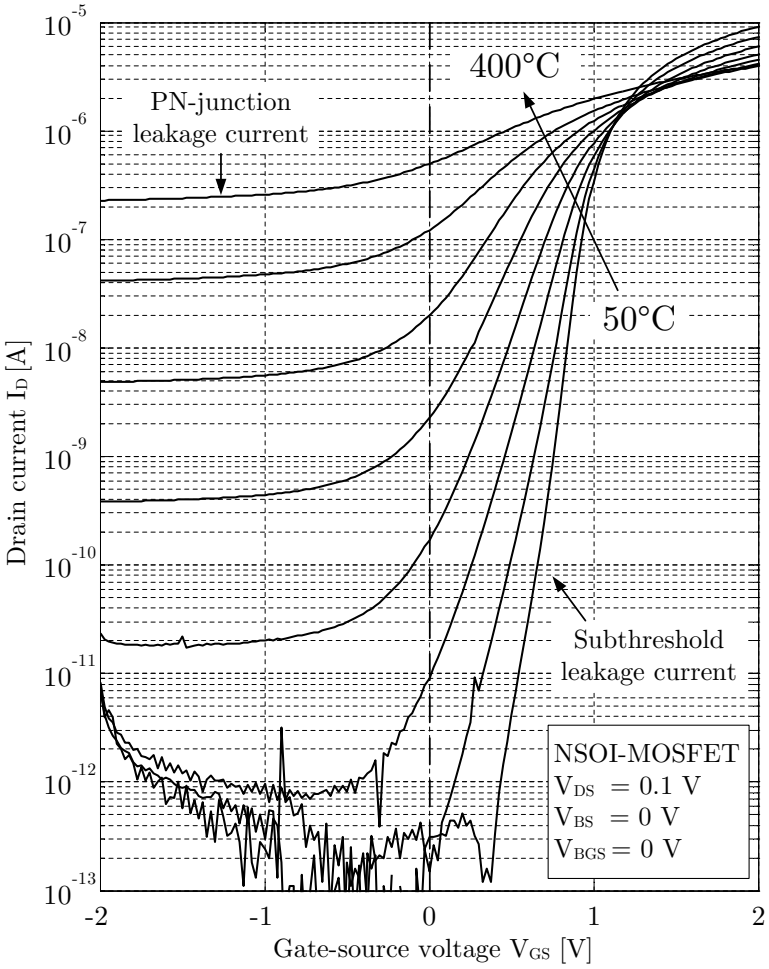

Figure 4.4: Weak inversion input characteristics of an N-channel SOI-MOSFET as a function of gate-source voltage V_{GS} for different temperatures from 50 °C up to 400 °C.

The measurements were carried out in a high temperature oven according to the measurement setup described in appendix A.2. A relatively high noise level can be recognized at low drain current levels, which is related to the measurement setup. The N-channel SOI-MOSFET has a channel width of 8 µm and a channel length of 4.8 µm. The overall device leakage current is defined as the current flowing into the drain terminal of the transistor, when the device is turned off by a zero gate-source voltage ($V_{GS} = 0\,\mathrm{V}$). At low temperatures up to 100 °C, the leakage current is lower than 1 pA. At 400 °C, the leakage current reaches 0.5 µA. It can be seen from Figure 4.4 that the leakage current at $V_{GS} = 0\,\mathrm{V}$ and for temperatures above 100 °C is an exponential function of the gate-source voltage V_{GS}. The reason for that is the change of inversion state, i.e. from depletion ($0 < \phi_{S1} < \phi_F$) to weak inversion ($\phi_F < \phi_{S1} < 2\phi_F$). This change is primarily initiated by the influence of increasing temperature, rather than by gate-source

voltage V_{GS}. The resulting main contributor to the overall leakage current is the subthreshold leakage current, which is increased due to weak inversion at high temperatures. Although the subthreshold leakage current dominates the leakage current at $V_{GS} = 0\,\mathrm{V}$ and high temperatures, the investigation of the PN-junction leakage current can be useful to verify the depletion state of the SOI-MOSFET device. Whether the PN-leakage current is dominated by the generation- or the diffusion mechanism inside the silicon film, can be recognized from the PN-junction leakage current's proportionality to n_i or n_i^2, respectively [Col04]. The PN-junction leakage current was measured over temperature in order to resolve this problem. To make sure no subthreshold channel current is measured at the drain of the transistor, the PN-junction leakage current was measured with a gate-source voltage of $V_{GS} = -1\,\mathrm{V}$. The resulting normalized PN-junction leakage current of an N-channel SOI-MOSFET with a drain-source voltage of $V_{DS} = 0.1\,\mathrm{V}$ and gate-source voltage of $V_{GS} = -1\,\mathrm{V}$ is shown in Figure 4.5. The intrinsic carrier concentrations n_i and n_i^2 were normalized ($n_i/10^{25}$, $n_i^2/10^{40}$) in order to compare their temperature gradient to the PN-junction leakage current, which is shown in Figure 4.5. The expression in Equation (3.3) was used for the calculation of n_i. The PN-junction leakage current is proportional to the square of the intrinsic carrier concentration n_i^2 at high temperatures above 150 °C. Since the PN-junction leakage current is proportional to n_i^2 at high temperatures, it can be assumed that the diffusion current is the dominating contributor to the PN-leakage current of partially depleted SOI-MOSFETs, which is also known from literature [Col04].

The investigation of leakage current mechanisms over temperature also proves that SOI-MOSFET devices in the considered SOI technology are partially depleted at high temperatures. Although PN-junction leakage currents are high, the subthreshold leakage current is the dominating portion of the overall leakage, which is measured at the drain of the devices at high temperatures.

4.4 SOI-MOSFET Performance

Besides the static leakage behavior of SOI-MOSFETs, also their dynamic performance characteristics, e.g. intrinsic gain and intrinsic bandwidth are crucial for analog circuit design at high temperatures. As an essential figures of merit for the analysis of intrinsic gain and intrinsic bandwidth, the g_m/I_d factor as well as the Early voltage V_A are investigated at high temperatures in the following section.

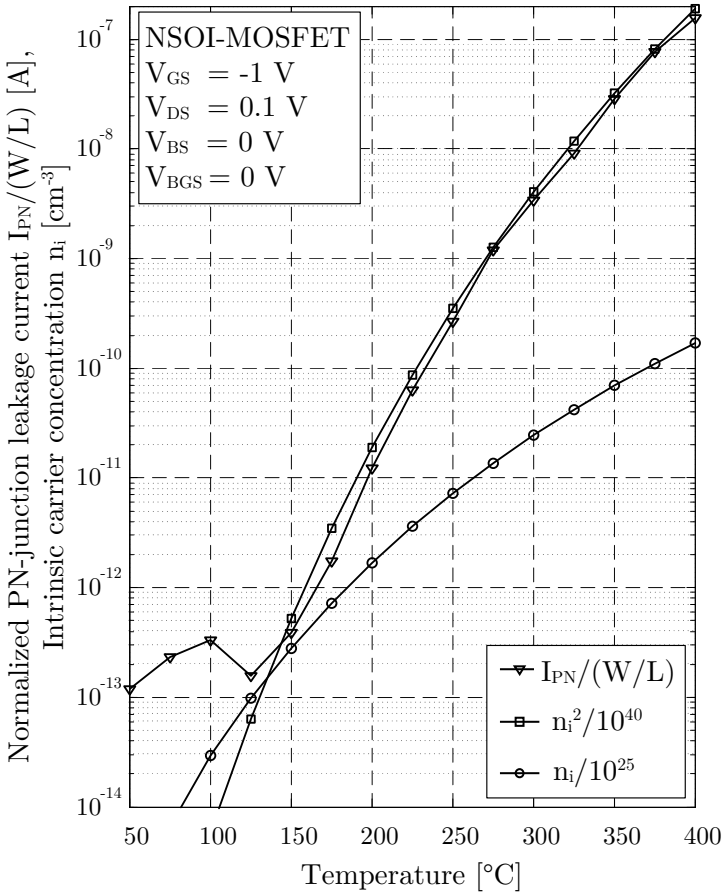

Figure 4.5: Measured normalized PN-junction leakage current of an N-channel SOI-MOSFET over temperature with $V_{GS} = -1\,\mathrm{V}$ and $V_{DS} = 0.1\,\mathrm{V}$.

4.4.1 g_m/I_d Factor at High Temperatures

An expression of the g_m/I_d factor in all regions of operation, i.e. from weak inversion to strong inversion, was discussed in Section 3.10.1 and is once again written in Equation (4.5).

$$\left.\frac{g_m}{I_d}\right|_{WI \to SI} = \frac{1}{nV_t\left(\sqrt{IC + 0.25} + 0.5\right)} \tag{4.5}$$

Due to the influence of the thermal voltage V_t, the transconductance efficiency decreases with increasing temperature. In addition, the transconductance efficiency also decreases with increasing inversion coefficient IC. The g_m/I_d factor in all regions of operation from weak inversion to strong inversion can be experimentally obtained from the input characteristics (I_d over V_{GS}) by performing the calculation given in Equation (4.6) [FKR10] [Jes10].

$$\frac{g_m}{I_d} = \frac{\partial I_d}{\partial V_{GS}} \cdot \frac{1}{I_d} = \frac{\partial ln(I_d)}{\partial V_{GS}} \tag{4.6}$$

Experimental results for the NHGATE SOI-MOSFET device are shown over normalized drain current $I_d/(W/L)$ for temperatures up to 400 °C in Figure 4.6. The film of the transistor was short-circuited with the source ($V_{BS} = 0\,\mathrm{V}$).

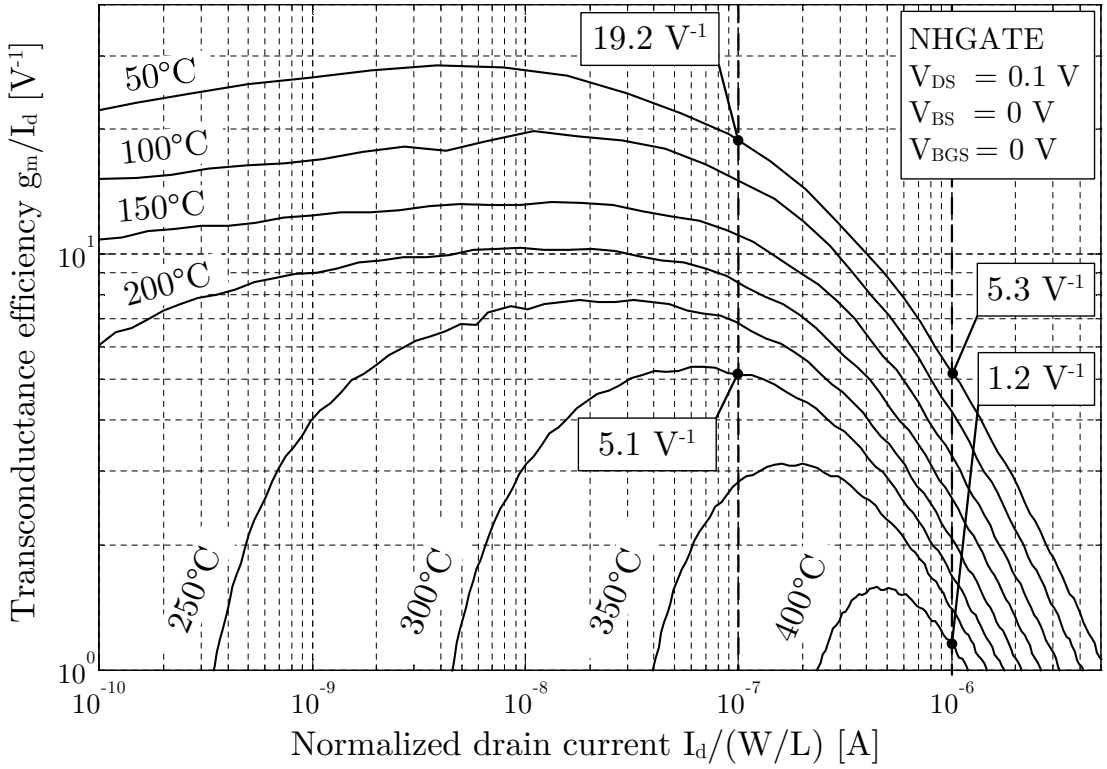

Figure 4.6: Measured transconductance efficiency g_m/I_d over normalized drain current $I_d/(W/L)$ for different temperatures with $V_{DS} = 0.1\,\mathrm{V}$, $V_{BS} = 0\,\mathrm{V}$ and $V_{BGS} = 0\,\mathrm{V}$.

Three main effects of increasing temperature on the level of transconductance efficiency can be distinguished from Figure 4.6. First of all, the g_m/I_d factor in weak inversion decreases due to the increase of thermal voltage V_t. This is the case for fully depleted as well as partially depleted devices. As a second effect, the body factor n increases with temperature, which further decreases the transconductance efficiency in weak inversion. As a third effect, leakage currents dominate the drain current of the device at high temperatures and result in a transconductance efficiency lower than $1\,\mathrm{V}^{-1}$. This can be explained as follows: If leakage currents are high, the drain current cannot be effectively controlled by the gate-source voltage. Thus, g_m tends towards zero. In addition, the drain current is

high due to leakage currents. This relationship is shown in Equation (4.7), where $I_d = I_{CH} + I_L$.

$$\frac{g_m}{I_d} = \frac{\partial\left(I_d\right)}{\partial V_{GS}} \cdot \frac{1}{I_d} = \frac{\partial\left(I_{CH} + I_L\right)}{\partial V_{GS}} \cdot \frac{1}{I_{CH} + I_L} \tag{4.7}$$

As I_L increases at high temperatures, the g_m/I_d factor tends towards zero for channel currents lower than the leakage current level.

The technology current is usually obtained graphically from the g_m/I_d measurement over normalized drain current $I_d/(W/L)$ by applying tangents in the weak inversion region and the strong inversion region, as is was shown in Figure 3.17 [Bin07b]. The intersection point of these two tangents is referred to as the center of the moderate inversion region [Bin07b]. As one can see in Figure 4.6, e.g. at a temperature of 250 °C, there is no consistent value of g_m/I_d in weak inversion. As a result, the technology current cannot be extracted as leakage currents affect the g_m/I_d factor at high temperatures. Nevertheless, a careful approximation of the technology current can be done by applying the tangent method at 50 °C. The approximate center of the moderate inversion region is thereby estimated to be in the range of 100 nA. In this case, the current range from 10 nA to 1 µA represents the moderate inversion region.

The g_m/I_d factor In the expected center of the moderate inversion region ($I_d/(W/L) = 100\,\text{nA}$), g_m/I_d for a temperature of 50 °C is equal to $19.2\,\text{V}^{-1}$. At temperatures higher than 300 °C, the g_m/I_d value is strongly affected by device leakage currents. In order to keep a sufficient safety margin to the leakage current level, the drain current must not be lower than ten times the leakage current level.

As a result, the moderate inversion region cannot be recommended for device operation at temperatures higher than 300 °C. The remaining g_m/I_d value at this temperature is $5.1\,\text{V}^{-1}$. A normalized drain current of 1 µA should be specified, in order to operate the device up to a temperature of 400 °C. According to the approximation of the moderate inversion region, the device then operates at the onset of strong inversion. The g_m/I_d values at this point are $5.3\,\text{V}^{-1}$ and $1.2\,\text{V}^{-1}$ for 50 °C and 400 °C, respectively. It is important to mention here that these measurements were taken with a drain-source voltage of $V_{DS} = 0.1\,\text{V}$. Since the subthreshold leakage current increases significantly for $V_{DS} \gg V_t$, a higher leakage current level is expected for higher drain-source voltages.

Figure 4.7 shows the measured g_m/I_d factor of PHGATE SOI-MOSFETs over normalized drain current $I_d/(W/L)$ for temperatures up to 400 °C with a drain-source voltage of $V_{DS} = -0.1\,\text{V}$, a body-source voltage of $V_{BS} = 0\,\text{V}$ and a back gate-source voltage of $V_{BGS} = -5\,\text{V}$. At a normalized drain current of

100 nA, which is the approximated center of moderate inversion, a g_m/I_d factor of $9\,V^{-1}$ was obtained at 50 °C. With respect to the leakage current level, the recommendable upper temperature for moderate inversion is 250 °C. Above 250 °C, leakage currents are significantly affecting the transconductance efficiency in the moderate inversion region. If it is necessary to operate the device up to a temperature of 400 °C, a normalized drain current higher than 1 µA should be specified.

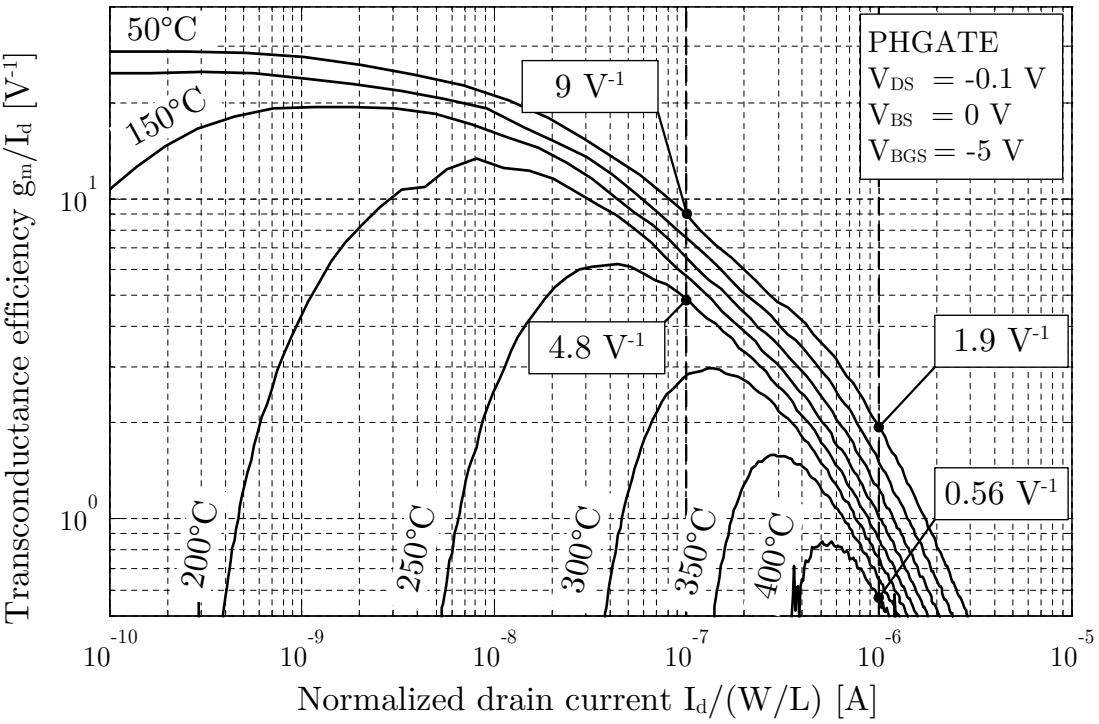

Figure 4.7: Measured transconductance efficiency g_m/I_d of a PHGATE SOI-MOSFET for different temperatures with $V_{DS} = -0.1\,V$, $V_{BS} = 0\,V$ and $V_{BGS} = -5\,V$.

These measurement results demonstrate that the transconductance efficiency factor g_m/I_d is strongly affected by device leakage currents. Similar results have also been obtained by [EHT+05]. The device operating currents have to be chosen carefully in order to keep a safety margin to the leakage current level, especially at temperatures above 250 °C. This restriction prohibits the use of moderate inversion at high temperatures. Since the devices can only be biased in strong inversion instead, the achievable overall transconductance efficiency of N-channel and P-channel SOI-MOSFETs is low compared to the values achievable in moderate inversion.

Up to this point, the technology current was estimated graphically to lie in the range of 100 nA. In the following section, its dependencies on temperature, as well as its dependency on the depletion state of the transistor device will be discussed.

4.4.2 Technology Current at High Temperatures

It was shown in the previous section that the technology current cannot be easily extracted at very high temperatures since the maximum weak-inversion value of the g_m/I_d factor is strongly affected by device leakage currents. In this section, the temperature dependency of the technology current is investigated further from a theoretical point of view, in order to estimate the technology current for partially depleted devices. The expression for the technology current was introduced in Section 3.10.2 and is given in (4.8) [Bin07b].

$$I_0(T) = 2\mu_0(T) C'_{OX1} n(T) V_t^2(T) \tag{4.8}$$

The technology current is dependent on the zero-field charge carrier mobility $\mu_0(T)$, as one can see from Equation (4.8). In case N-channel SOI-MOSFETs are considered, electrons in the inverted channel form the overall channel current. The zero-field charge carrier mobility of electrons as a function of temperature can be written as given in (4.9) [SN07].

$$\mu_0(T) = \mu_{T0} \left(\frac{T}{T_0} \right)^{\mathrm{BEX}} \tag{4.9}$$

In Equation (4.9), BEX is the mobility temperature exponent. A zero-field charge carrier mobility factor $\mu_{T0} = 1000\,\mathrm{cm}^2/\mathrm{Vs}$ was used for a doping concentration of $N_{CH} = 3 \cdot 10^{16}\,\mathrm{cm}^{-3}$ and $T_0 = 300\,\mathrm{K}$ [SN07]. The mobility temperature exponent BEX is expected to be in the range of -1.9 for N-channel SOI-MOSFET devices and -1.6 for P-channel SOI-MOSFET devices [Wer96]. These values were taken from [Wer96] and were obtained from a SIMOX (Separation by implantation of oxygen) technology with similar device dimensions and threshold voltages. The mobility of electrons is also dependent on the inversion level and the drain-source voltage V_{DS}. This dependency is neglected for simplicity. The temperature dependency of the body factor $n(T)$ in a partially depleted SOI-MOSFETs is determined by the depletion depth x_{d1} and is given by

$$n|_{PD}(T) = 1 + \frac{\epsilon_{si}}{x_{d1}(T) C'_{OX1}} = 1 + \frac{\epsilon_{si}}{\sqrt{\frac{2\epsilon_{si}\phi_{S1}(T)}{qN_A}} C'_{OX1}}\,, \tag{4.10}$$

in which the front gate surface potential $\phi_{S1}(T)$ is the only temperature dependent factor. In weak inversion, ϕ_{S1} is higher than the Fermi potential but lower than twice the Fermi potential. In moderate inversion, ϕ_{S1} is higher than twice the Fermi potential but lower than $2\phi_F + \Delta\phi$, and in strong inversion its higher than $2\phi_F + \Delta\phi$ [TM11].

$$\phi_{S1} = \begin{cases} \phi_F \ldots 2\phi_F & \text{in weak inversion} \\ 2\phi_F \ldots (2\phi_F + \Delta\phi) & \text{in moderate inversion} \\ > (2\phi_F + \Delta\phi) & \text{in strong inversion} \end{cases} \tag{4.11}$$

Since $\Delta\phi$ varies between $0 \ldots 7V_t$ [TM11], a front gate surface potential of $2\phi_F$ is expected in moderate inversion. The technology current can then be rewritten as

$$I_0(T) = 0.1\,\mathrm{m}^2/\mathrm{Vs} \cdot \left(\frac{T}{300K}\right)^{BEX} \left(C'_{OX1} + \epsilon_{si}\sqrt{\frac{qN_A}{4\epsilon_{si}\phi_F(T)}}\right)\left(\frac{kT}{q}\right)^2 . \tag{4.12}$$

The qualitative technology current I_0 over temperature, calculated from Equation (4.12), is depicted in Figure 4.8 for partially- and fully depleted SOI-MOSFETs.

In case the device is partially depleted, the temperature dependency of the body factor dominates the overall temperature dependency of the technology current. It should be noted from Figure 4.8 that the temperature coefficient of the technology current in a fully depleted SOI-MOSFET is mainly determined by the thermal voltage V_t and the zero-field carrier mobility μ_0. The first order temperature coefficient of the mobility varies dependent on many technology parameters [SN07][TM11], and cannot be defined in general at this point. Thereby, it is expected for fully depleted devices that both dependencies almost cancel each other out. In case the temperature exponent of the zero-field charge carrier mobility BEX is smaller than -2, the overall temperature coefficient of the technology current will be negative.

From a circuit design point of view, the increase in technology current with temperature results in a shift of the moderate inversion region to higher current densities. If the transistor is biased in the lower moderate inversion region, with a temperature independent drain current, the transistor can enter weak inversion only by the influence of increased temperature.

The technology current cannot be easily extracted at high temperatures, as already discussed before. Since leakage currents dominate the weak inversion

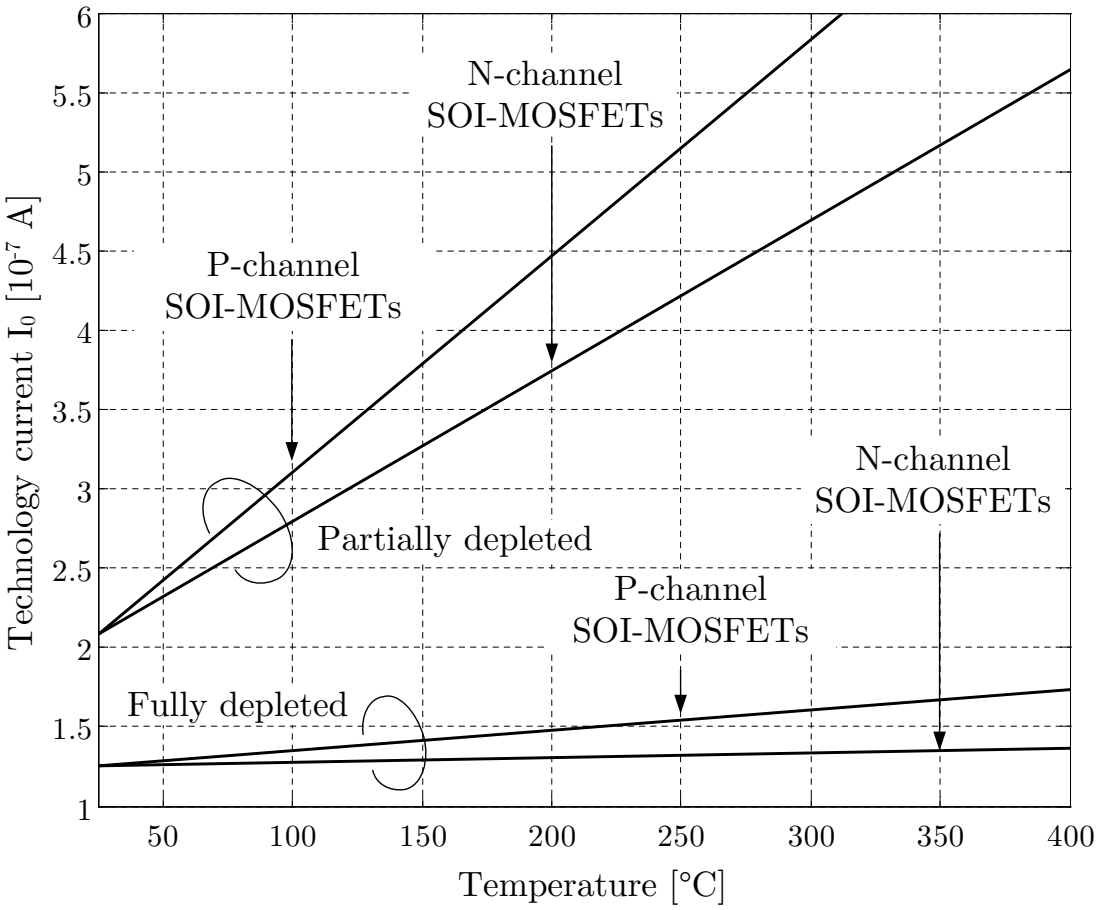

Figure 4.8: Calculated technology current I_0 of partially depleted and fully depleted SOI-MOSFETs over temperature. In the partially depleted case, the influence of the body factor n dominates the overall temperature dependence of the technology current.

region, the weak inversion tangent cannot be applied to the measured curves in order to find the technology current. A fitting technique to solve this issue has been proposed by [EHT+05]. The technique uses the expression of the g_m/I_d factor in all regions of inversion which is given in Equation (4.13) [EHT+05].

$$\frac{g_m}{I_d}\,(\text{fit}) = \left[n\,(\text{fit})\, V_t \left(\sqrt{\frac{I_d}{I_0\,(\text{fit})\,(W/L)} + 0.25} + 0.5 \right) \right]^{-1} \tag{4.13}$$

The body factor $n\,(\text{fit})$ and the technology current $I_0\,(\text{fit})$ are used as fitting parameters. A variation of the technology current I_0 shifts the g_m/I_d curve on the x axis, whereby a change in body factor n shifts the curve on the y axis. For the fitting technique proposed by [EHT+05], both fitting parameters are chosen so that the fitted curve matches the measured curve in strong inversion. Furthermore it is assumed that the body factor n is independent on temperature

[EHT+05]. With this simplification, the technology current I_0 can be extracted at high temperatures. The method is accurate in a lower temperature range, since it only fits the g_m/I_d factor in strong inversion where leakage currents have a decreased influence [EHT+05]. Nevertheless, n has been assumed constant for temperatures above 50 °C in [EHT+05] [Bin07b]. In this work, the body factor of partially depleted SOI-MOSFETs cannot be assumed constant over temperature, as it has been discussed before. Figure 4.9 shows the proposed fitting technique for the considered NHGATE SOI-MOSFET at 200 °C and 300 °C.

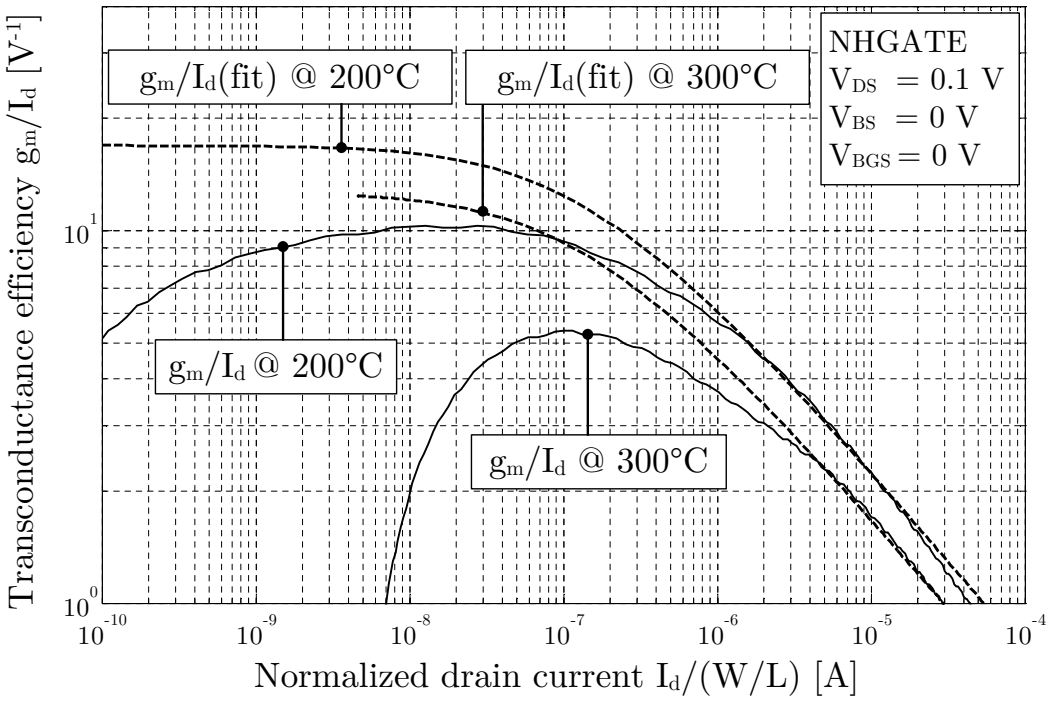

Figure 4.9: Measured (solid) and fitted (dotted) g_m/I_d factor over normalized drain current $I_d/(W/L)$ at 200 °C and 300 °C.

Due to the fact that n is not constant with temperature for partially depleted devices, the g_m/I_d curve can be fitted with multiple values of n and I_0. The technology current I_0 can therefore not be extracted explicitly, since n is unknown. As a consequence, the proposed fitting technique can be only applied to fully depleted SOI-MOSFETs, for which n varies only slightly with temperature.

4.4.3 Early Voltage at High Temperatures

The Early voltage is an important analog design parameter for applications where high output resistance of SOI-MOSFET devices is required. Usually, the Early

voltage can be considered independent on the drain-source voltage. However, within this work, the drain-source voltage is always stated for a given Early voltage, which is especially useful when the Early voltage is characterized as a function of drain current.

In the following consideration, the Early voltage is extracted for two different drain-source voltages, i.e. for $V_{DS} = 2\,\mathrm{V}$ and $V_{DS} = 4\,\mathrm{V}$. Figure 4.10 shows the drain current I_d over V_{DS} of an NHGATE SOI-MOSFET. The two drain-source voltage extraction points are marked as dashed lines for gate-source voltages of $V_{GS} = 0\,\mathrm{V} \ldots 5\,\mathrm{V}$. The operating temperature is 150 °C, the body-source voltage is $V_{BS} = 0\,\mathrm{V}$ and the back gate-source voltage is $V_{BGS} = 0\,\mathrm{V}$.

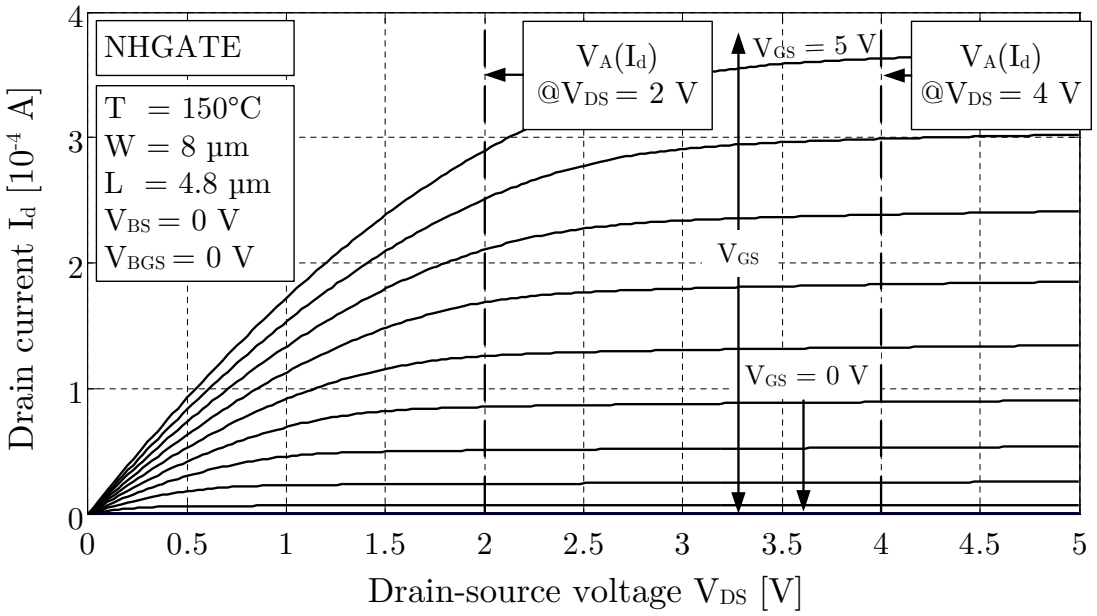

Figure 4.10: Measured drain-source current I_d of an NHGATE SOI-MOSFET with channel length of 4.8 µm and a channel width of 8 µm at 150 °C.

For the following experimental investigation, the gate-source voltage is varied with a step size of $\Delta V_{GS} = 25\,\mathrm{mV}$. For better visibility, a reduced number of output curves are shown in Figure 4.10. By increasing V_{GS} in small step sizes, the Early voltage as a function of drain current can be obtained from the expression presented in Equation (4.14) [FKR10] [Jes10].

$$V_A = \frac{I_d}{g_{ds}} = \left(\frac{\partial I_d}{\partial V_{DS}} \cdot \frac{1}{I_d} \right)^{-1} = \left(\frac{\partial ln(I_d)}{\partial V_{DS}} \right)^{-1} \tag{4.14}$$

The Early voltages of a Split-Source NSOI device and an NHGATE device at a temperature of 350 °C are now shown in Figures 4.11 a) and 4.11 b). The film of the NHGATE device was short-circuited with source ($V_{BS} = 0\,\mathrm{V}$). The

drain-source voltages are $V_{DS} = 2\,\mathrm{V}$ and $V_{DS} = 4\,\mathrm{V}$ for Figures 4.11 a) and 4.11 b), respectively.

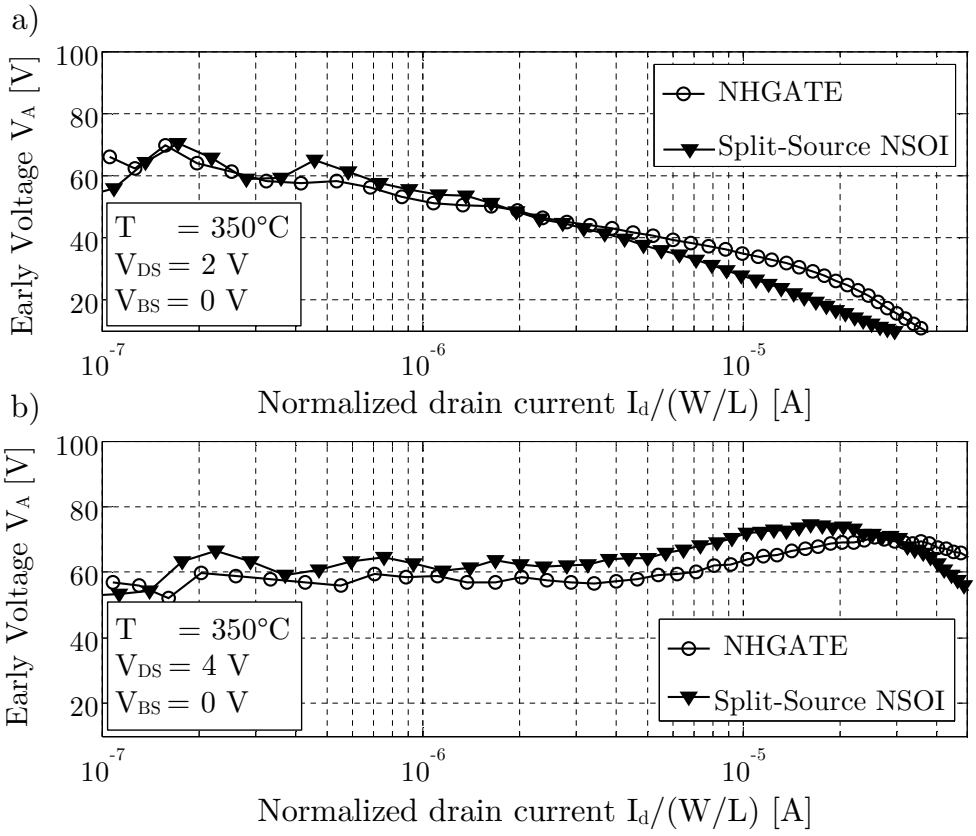

Figure 4.11: Measured Early voltage V_A as a function of normalized drain current $I_d/(W/L)$ of a Split-Source NSOI-MOSFET and an NHGATE SOI-MOSFET at 350 °C with a) a drain-source voltage of $V_{DS} = 2\,\mathrm{V}$ and b) with a drain-source voltage of $V_{DS} = 4\,\mathrm{V}$.

It can be seen in Figure 4.11 a) that the Early voltage is approximately 60 V in the lower drain current range. The Early voltage decreases as V_{DS} approaches V_{DSsat} in the higher drain current range [Bin07b]. If the temperature increases further up to 400 °C, as shown in Figure 4.12, leakage currents tend to increase and reach the level of the operating current in moderate inversion. At this temperature, the leakage current level is approximately 300 nA . . . 400 nA, which limits the minimum achievable operating current of the device. The operating current should be significantly higher than the leakage current level in case it is intended to operate the device up to this temperature.

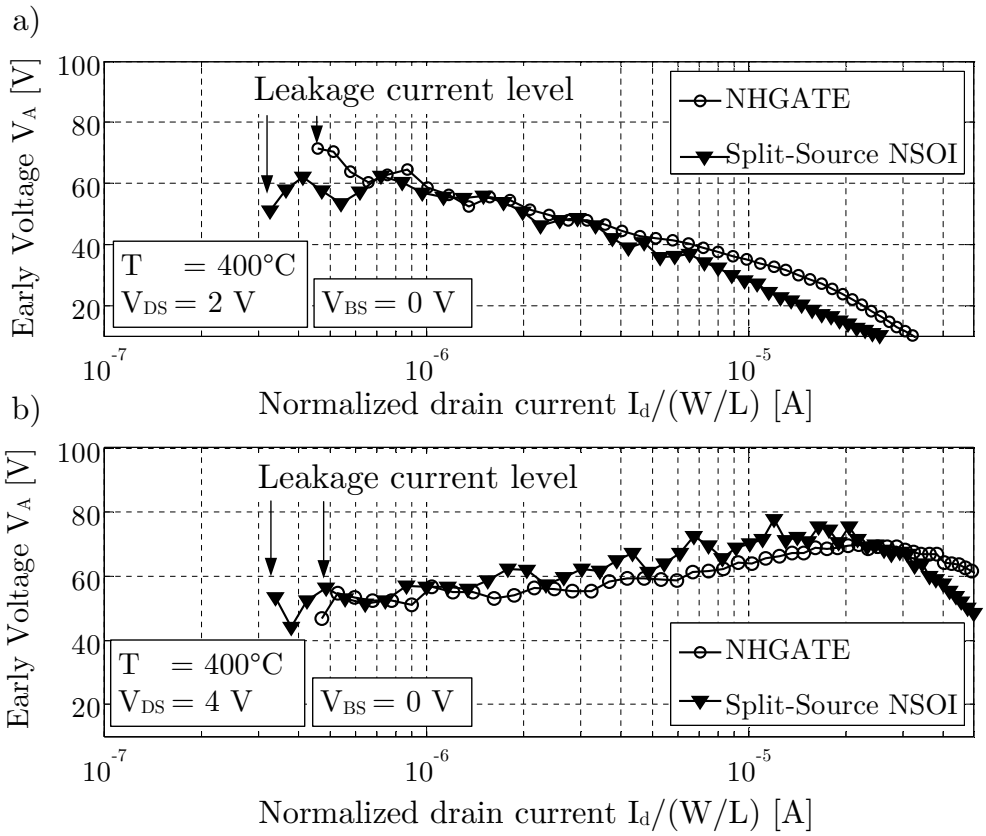

Figure 4.12: Measured Early voltage V_A as a function of normalized drain current $I_d/(W/L)$ of a Split-Source NSOI-MOSFET and an NHGATE SOI-MOSFET at 400 °C with a) a drain-source voltage of $V_{DS} = 2\,\mathrm{V}$ and b) with a drain-source voltage of $V_{DS} = 4\,\mathrm{V}$.

4.4.4 Intrinsic Gain at High Temperatures

The temperature dependency of the intrinsic gain of HGATE SOI-MOSFET devices is investigated in this section. For an common source gain stage with ideal current source load, the intrinsic gain can be written as [Bin07b]

$$A_i = -g_m \cdot r_{ds} = -\frac{g_m}{g_{ds}} = -\left(\frac{g_m}{I_d}\right) V_A \,. \tag{4.15}$$

After Equation (4.15), the intrinsic gain can be obtained by the multiplication of the g_m/I_d factor with the Early voltage. The expression is accurate in case the drain-source voltage V_{DS} is stated for the Early voltage [Bin07b]. Intrinsic gain of NHGATE and PHGATE SOI-MOSFETs was obtained experimentally. In Figure 4.13, the intrinsic gain of NHGATE SOI-MOSFETs over drain current is shown for different temperatures from 50 °C to 400 °C with a drain-source voltage of $V_{DS} = 3\,\mathrm{V}$, a body-source voltage of $V_{BS} = 0\,\mathrm{V}$ and a back gate-source voltage of $V_{BGS} = 0\,\mathrm{V}$.

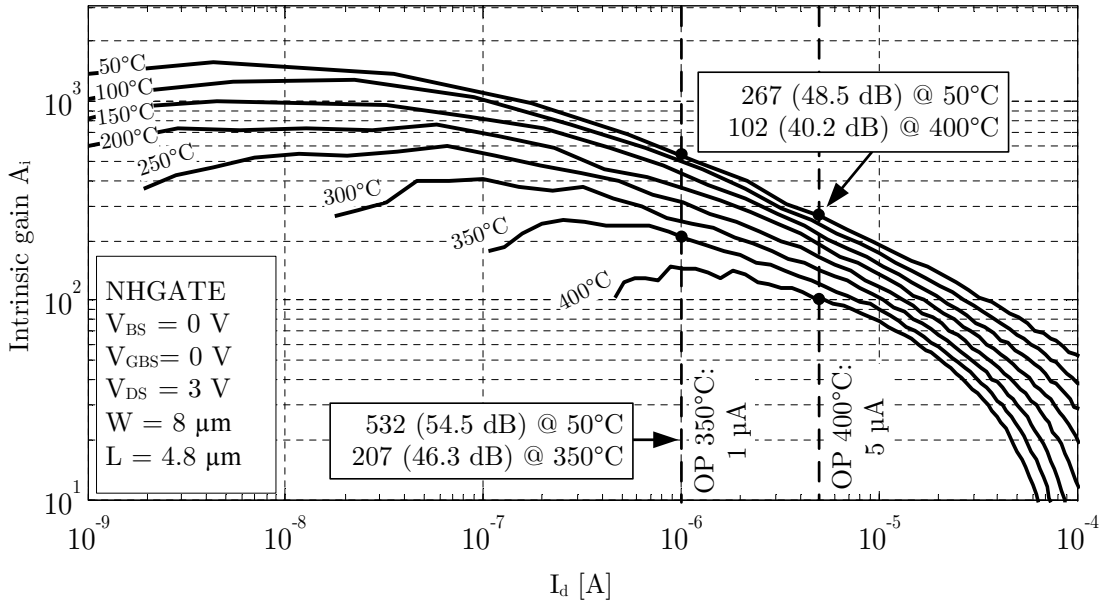

Figure 4.13: Intrinsic gain of NHGATE SOI-MOSFETs over drain current I_d for a drain-source voltage of $V_{DS} = 3\,\mathrm{V}$ and temperatures from 50 °C up to 400 °C.

As the transconductance efficiency g_m/I_d decreases with increasing drain current, also the intrinsic gain decreases. A drain current significantly higher than the leakage current level should be chosen in order to keep a safety margin to the leakage current level in a high temperature design approach. Therefore, a drain current of approximately 5 µA is necessary to operate the device up to 400 °C. At this specific operating current, the intrinsic gain is 48.5 dB at 50 °C and 40.2 dB at 400 °C. In case an upper operating temperature limit of 350 °C is defined, a minimum drain current of 1 µA is required to operate the device. Due to the increase of intrinsic gain with decreasing operating current densities, gain values of 54.5 dB and 46.3 dB can be reached at 50 °C and 350 °C, respectively.

Figure 4.14 illustrates the intrinsic gain of PHGATE SOI-MOSFETs over drain current for different temperatures up to 400 °C. The PHGATE device is biased with a drain-source voltage $V_{DS} = -3\,\mathrm{V}$ and a body-source voltage of $V_{BS} = 0\,\mathrm{V}$ according to the regular operation in analog circuits. The back gate-source voltage is $V_{BGS} = -5\,\mathrm{V}$. It can be seen from Figure 4.14 that the intrinsic gain is decreased significantly, as temperature increases. If the device is operated up to 400 °C, the minimum drain current with respect to the leakage current level is approximately 7 µA. These results demonstrate the significant impact of operating temperature on the intrinsic gain of SOI-MOSFETs. Adequate intrinsic gain values for analog circuit design can be achieved in the moderate inversion region. Therefore, the

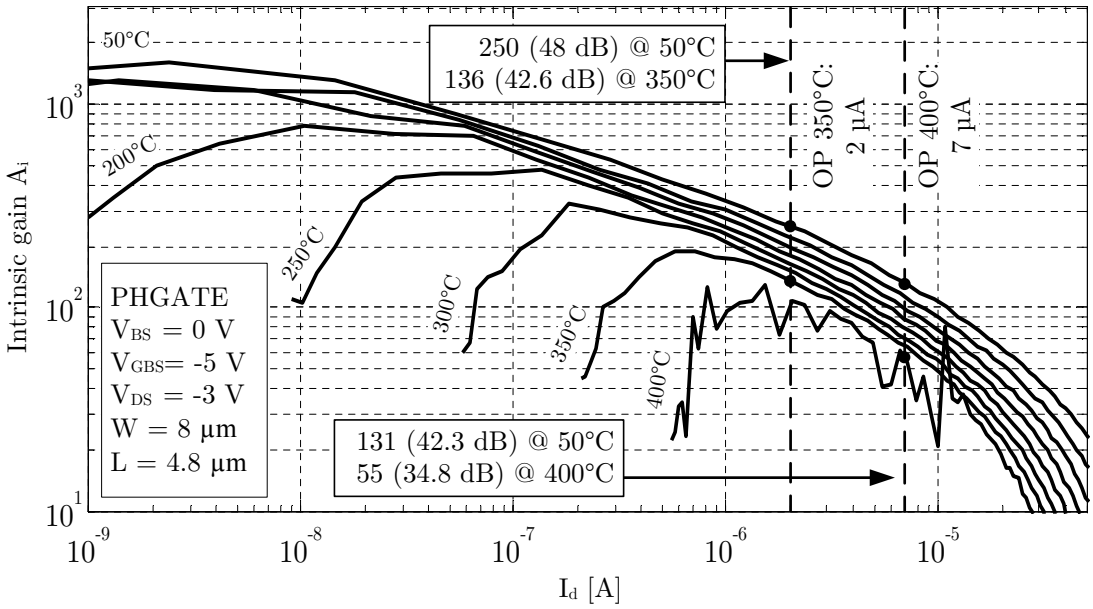

Figure 4.14: Intrinsic gain of PHGATE SOI-MOSFETs over drain current I_d for a drain-source voltage of $V_{DS} = -3\,\mathrm{V}$ and temperatures from 50 °C up to 400 °C.

moderate inversion region is a desired point of operation for sufficient intrinsic gain and bandwidth. Due to increased leakage currents at high temperature, the g_m/I_d factor and the intrinsic gain A_i are significantly decreased. As a result, SOI-MOSFETs can only be operated in strong inversion at very high operating temperatures. Especially in applications, where high gain levels are required, e.g. in switched capacitor circuits, the operating point of strong inversion limits the achievable accuracy due to decreased intrinsic gain.

4.4.5 Intrinsic Bandwidth at High Temperatures

The intrinsic bandwidth or cutoff frequency of an SOI-MOSFET is given by [Bin07b]

$$f_T = \left(\frac{IC}{\left(\sqrt{IC + 0.25} + 0.5\right)} \right) \left(\frac{\mu_0 V_t}{\pi \left(\hat{C}_{GSi} + \hat{C}_{GBi} \right) L^2} \right) . \tag{4.16}$$

The sum of the normalized intrinsic gate-source capacitance $\hat{C}_{GSi}$ and the normalized intrinsic gate-film capacitance $\hat{C}_{GBi}$ is defined differently for moderate inversion and strong inversion, and is given in (4.17) and (4.18), respectively [Bin07b].

$$\left(\hat{C}_{GSi} + \hat{C}_{GBi}\right)\Big|_{MI} = \frac{n - 2/3}{n} \tag{4.17}$$

$$\left(\hat{C}_{GSi} + \hat{C}_{GBi}\right)\Big|_{SI} = \frac{n - 1/3}{n} \tag{4.18}$$

Using Equation (4.17), the intrinsic bandwidth in the moderate inversion region can be rewritten as

$$f_T = \left(\frac{IC}{\left(\sqrt{IC + 0.25} + 0.5\right)}\right)\left(\frac{n\mu_0 V_t}{(n - 2/3)\,\pi L^2}\right). \tag{4.19}$$

It can be seen from Equation (4.19) that the device length L has to be minimized in order to maximize the intrinsic bandwidth of the device. The moderate inversion region offers a good compromise between achievable intrinsic gain and intrinsic bandwidth. In this region, the dependency of intrinsic bandwidth on temperature is mainly determined by the zero-field charge carrier mobility μ_0, the body factor n, and the thermal voltage V_t. If the device is biased with a constant operating current, the inversion coefficient increases with increasing temperatures, which is due to the increase of the body factor n in partially depleted SOI-MOSFETs. The intrinsic bandwidth of fully depleted SOI-MOSFETs is higher since n is smaller for these devices.

The intrinsic bandwidth of an N-channel SOI-MOSFET over temperature in partially depleted and fully depleted condition, calculated using Equation (4.19) with a channel length of $L = 4.8\,\mu\text{m}$ in moderate- and strong inversion is shown in Figure 4.15.

The intrinsic bandwidth of fully depleted SOI-MOSFETs, operating in moderate inversion is approximately 2.7 times higher compared to the intrinsic bandwidth of partially depleted devices. The factor increases further with increasing operating temperature. At 400 °C, the intrinsic bandwidth of a fully depleted SOI-MOSFET is 4.7 times higher compared to partially depleted SOI-MOSFETs.

It can be seen from these theoretical considerations that fully depleted SOI-MOSFETs show increased intrinsic bandwidth also at high temperatures. The moderate inversion region is the desired point of operation to achieve adequate intrinsic gain values combined with moderate intrinsic bandwidth. In this region, the intrinsic bandwidth is increased by a factor of 2.7 . . . 4.7 when the depletion state of the device is changed from partially depleted to fully depleted.

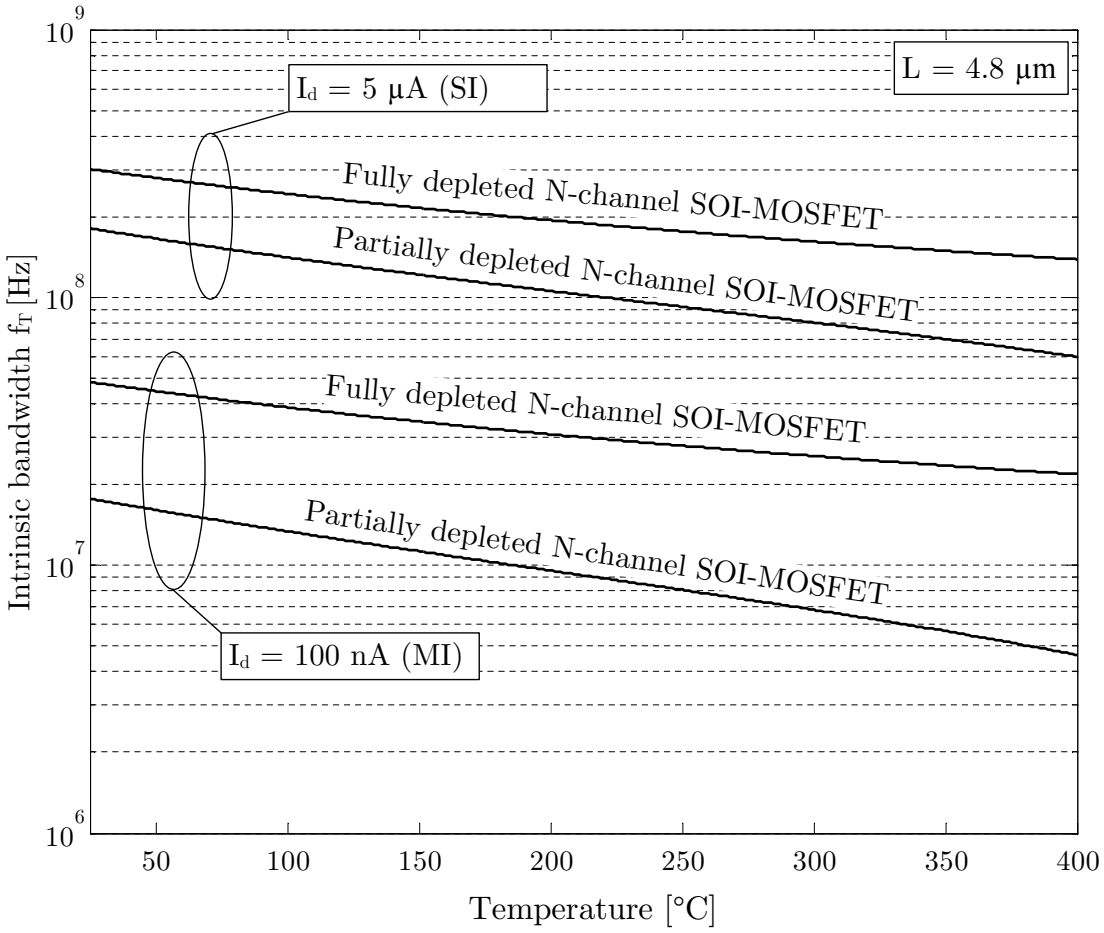

Figure 4.15: Calculated intrinsic bandwidth of partially depleted and fully depleted N-channel SOI-MOSFETs over temperature with a channel length of $L = 4.8\,\mu m$ in moderate- and strong inversion.

4.5 I_{ON}/I_{OFF} Ratio

In order to maximize the operation speed of digital and analog circuits, it is preferred to achieve a high I_{ON} current, whereby a low I_{OFF} current is also preferred for low static current consumption. With high I_{ON}/I_{OFF} ratios, transistors comprise low leakage currents and dissipate less power in case they are turned off. At the same time, they can achieve high drive currents when turned on by the maximum gate-overdrive voltage $(V_{GS1} - V_{th})$. The maximum on-state saturation current I_{dsat} of a N-channel SOI-MOSFET device can be written as (4.20) [Col04].

$$I_{dsat} = \frac{\mu_0 C'_{OX1}}{2n} \left(\frac{W}{L}\right) (V_{GS1} - V_{th})^2 \tag{4.20}$$

The maximum saturation current can be achieved at the maximum gate-source voltage. It can be seen from Equation (4.20) that the saturation current can also be increased by decreasing the threshold voltage of the device. For high temperature applications, a decreased threshold voltage cannot easily be realized. The reduction of the threshold voltage increases the maximum on-state current, but at the same time it also increases the off-state current of the device due to leakage currents. The I_{ON}/I_{OFF} ratios of NHGATE and PHGATE SOI-MOSFETs in the considered SOI technology were investigated over temperature and are shown in Figure 4.16.

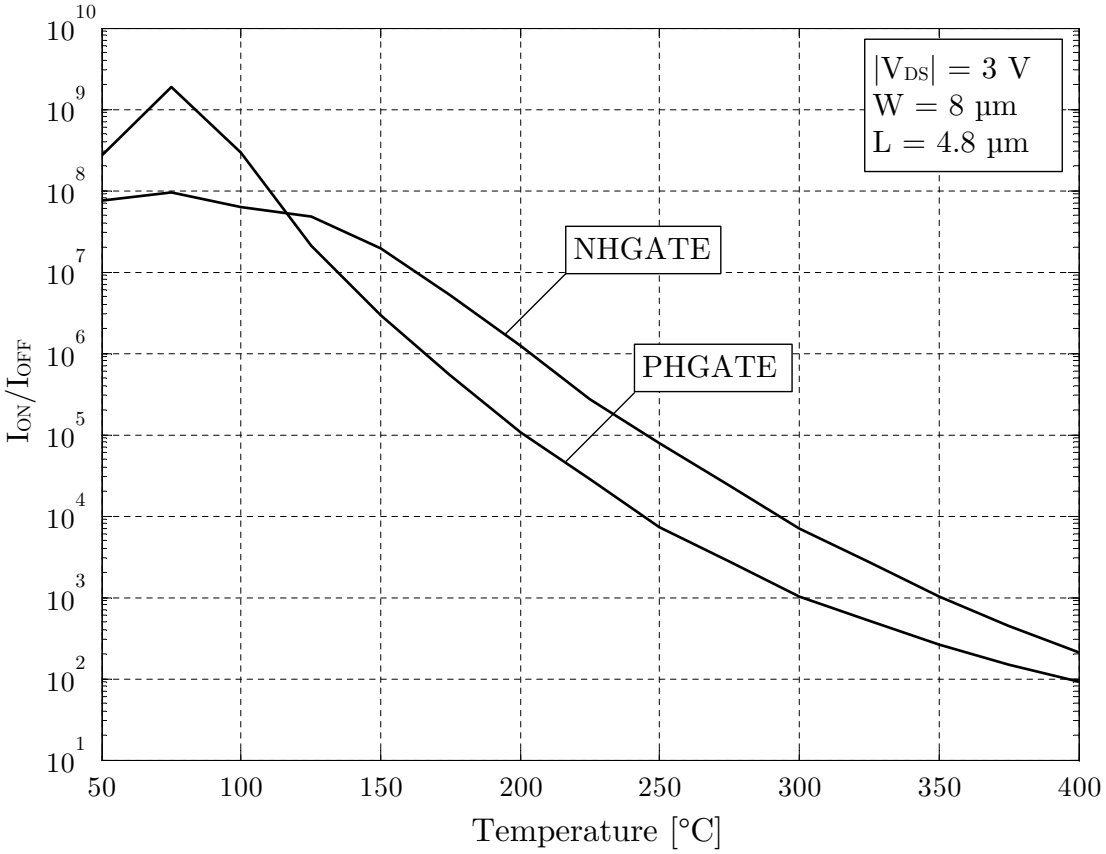

Figure 4.16: I_{ON}/I_{OFF} ratios of N-channel and P-channel HGATE SOI-MOSFET devices over temperature.

A high drain-source voltage of $|V_{DS}| = 3\,\mathrm{V}$ was chosen for the measurement in order to consider the subthreshold leakage current in off-state and to ensure that the device is in saturation in the on-state. At a drain-source voltage of $|V_{DS}| = V_{DDA}$, the I_{ON}/I_{OFF} ratio can be expected a little bit higher due to channel length modulation.

Fist of all, the I_{ON}/I_{OFF} ratio of both devices decreases over temperature, which is related to the strong influence of the zero-field charge carrier mobility

μ_0 on the saturation current of both devices. The I_{ON}/I_{OFF} ratio of N-channel devices is higher due to higher zero-field charge carrier mobility. The increased back gate effect of P-channel devices leads to decreased threshold voltage and thereby to an increase in saturation current. At the same time, a decreased threshold voltage also increases the off-state current of the device. In summary it can be concluded at this point that a significant reduction of the I_{ON}/I_{OFF} ratio at high temperatures was measured for both N-channel and P-channel SOI-MOSFETs.

4.6 Summary

In this section, the threshold voltages, leakage currents and essential analog performance parameters, i.e. the g_m/I_d factor, the technology current I_0, the Early voltage V_A as well as intrinsic gain and bandwidth were discussed in detail. It was shown that device leakage currents of SOI-MOSFETs increase significantly with increasing temperatures. The subthreshold leakage current is the dominating leakage current contributor at high temperatures and is mainly caused by a low threshold voltage at high temperatures. Since the threshold voltage exhibits a non-linear decrease with increasing temperature, it reaches very low values of around 0 V for both, N-channel and P-channel SOI-MOSFETs, which results in a significant increase of the subthreshold leakage current.

In addition, the intrinsic performance of the SOI-MOSFETs is decreased with increasing temperature. The performance loss can also be related to increasing leakage currents. The g_m/I_d factor is significantly affected by the increase of leakage currents, especially in the weak inversion region and the moderate inversion region. As a result, operation in the moderate inversion region is not feasible at high temperatures. Only the strong inversion region remains for safe operation at high temperatures, even for devices where high gain instead of high bandwidth is required. Analog circuits for applications where high DC gain is the primarily requirement, cannot be realized in PD-SOI technology without additional measures at temperatures up to 400 °C.

Chapter 5

Analog Circuits in a Wide Temperature Range

The influence of increasing temperature on the device characteristics of partially depleted and fully depleted SOI-MOSFETs were described in the previous chapters. It was demonstrated that the transition from fully to partially depleted with increasing temperature has a significant influence on the analog device characteristics. A summary of these effects is given in the following enumeration:

1. The depletion state of SOI-MOSFETs changes with temperature and bias voltage conditions, i.e. gate-source voltage, drain-source voltage and back gate-source voltage.

2. The non-linear decrease of threshold voltage leads to low threshold voltage values in the range of 0 V at high temperatures for both N-channel and P-channel SOI-MOSFETs.

3. Leakage currents increase mainly due to the decrease of threshold voltage. The PN-junction leakage current and the subthreshold leakage current also increase with increasing SOI-MOSFET device width. As a result, devices with large device widths, e.g. for applications where good matching or moderate inversion is required, are critical at high temperatures.

4. A ZTC (Zero-Temperature-Coefficient) point is not present due to the transition from partially depletion to fully depletion with increasing temperature. Analog circuits, which rely on the use of the ZTC bias point, e.g. ZTC voltage reference circuits, cannot be realized with sufficient accuracy.

5. The transconductance efficiency factor g_m/I_d decreases significantly due to leakage currents, especially in weak- and moderate inversion. As a

consequence, SOI-MOSFET devices can only be operated in strong inversion at high operating temperatures.

6. As shown in Section 4.4.2, the technology current I_0 cannot be extracted from g_m/I_d measurements of partially depleted SOI-MOSFETs. Since the body factor n is not constant in the considered temperature range, improved extraction techniques are required in order to extract the technology current experimentally. Knowledge of the technology current also provides the exact operating current density for operation in the center of the moderate inversion region.

7. The Early voltage cannot be determined for channel currents lower than the leakage current level as leakage currents dominate the overall device current in that region.

8. The intrinsic gain of SOI-MOSFETs decreases and tends towards 0 dB in the moderate inversion region as leakage current levels are approaching the operating current level. At high temperatures, the devices can only be operated in strong inversion, which results in a low overall intrinsic gain, also for applications where a high DC gain is required.

The impact of these issues on analog circuits is subdivided into static errors, induced by leakage currents and errors caused by the degradation of the SOI-MOSFET's analog small signal performance, e.g. intrinsic gain and intrinsic bandwidth. In the enumeration above, the effects 1-3 lead to static errors due to increased leakage current and also to malfunctions caused by low threshold voltages. The absence of a ZTC point, as described by number 4, does not allow the use of ZTC voltage references in analog circuits. Effects listed with numbers 5-8 cause errors which result from insufficient gain, e.g. in operational amplifiers or operational transconductance amplifiers for switched capacitor applications. It is important to mention here that these effects are a consequence of effects 1-3. Thereby, minimizing the effects 1-3 will also result in the minimization of the effects 4-8.

The impact on basic analog building blocks, e.g. basic current mirrors, analog switches, two-stage operational amplifiers and bandgap voltage references is investigated in the following section. The static and dynamic errors of these circuits have a high influence on almost every system assembled with these sub-circuits.

5.1 Fundamental Analog Building Blocks

The realization of complex integrated circuits, e.g. microprocessors, sensors or memories, also requires the utilization of analog circuitry. Within these complex systems, analog circuits are required, e.g. to generate clock signals for digital circuits, to convert analog signals to digital signals or to generate on-chip supply voltages. Thereby, the use of analog circuits is also necessary for the realization of digital systems. As a matter of fact, the operation of almost every integrated circuit, whether it is analog or mixed-signal, is strongly dependent on the performance of analog circuits.

In order to consider analog circuits in a more common approach, a set of very fundamental analog circuits has been assembled. The choice of basic analog circuits also agrees with the considerations made by [Kir98], where the improvement of these circuits has been stated as one of the most important long term research needs in high temperature electronics. These are:

- Analog switches
- Current mirrors
- Basic gain stages, i.e. common source, common drain and common gate amplifiers
- Operational amplifiers
- Voltage references

These fundamental analog circuits are inevitable for the realization of almost any considerable analog system. With the investigation of these analog circuits, also complex circuits comprised of these basic sub-circuits are thereby considered in this in work.

5.1.1 Analog Switches

Analog switched are widely used, e.g. in switched capacitor applications or input selection multiplexers in analog-digital-converters [SKK12]. Especially in switched capacitor application, leakage currents of the integrated switches can lead to errors as charges leak off or onto storage capacitors. In order to reduce the error in these circuits, capacitor sizes and switching speeds have to be increased. Increasing die area leads to increased cost per die and is therefore not a preferred solution. To target high switching speeds in switched capacitor circuits, high bandwidth

operational transconductance amplifiers are necessary. High bandwidth for these amplifiers can only be reached with high bias currents and small device dimensions, which results in decreased open loop DC gain [Bin07b]. Decreased open loop DC gain results in high gain errors within these circuits and thereby in decreased accuracy for high precision applications. In case low leakage switches are available, the bandwidth of transconductance amplifiers can be reduced to increase the accuracy. The reduction of leakage currents in analog switches is the preferred approach and focused in this work. Figure 5.1 shows a schematic of a symmetrical analog switch, consisting of HGATE transistors M_1-M_2 and charge injection compensation transistors M_3-M_6. The length and width of M_1 and M_2 are 4.8 µm and 9.6 µm, respectively. The width of the compensation transistors is 4.8 µm.

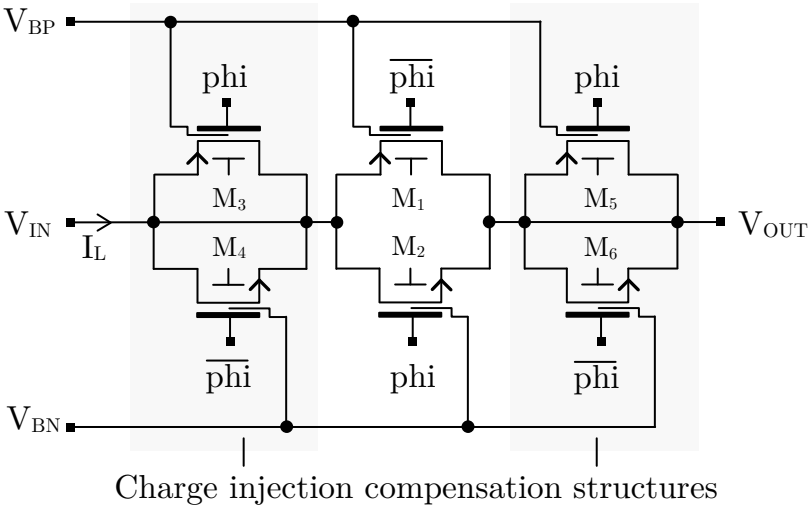

Figure 5.1: Schematic view of a symmetrical analog switch, composed of HGATE SOI-MOSFET devices including charge injection compensation structures.

Figure 5.2 shows a photograph of the switch in the considered SOI-CMOS technology.

As the switch is turned off, charges located in the channel of M_1 and M_2 are transferred to the channel of the compensation structures, as they are turned on. With the use of these charge injection compensation structures, the error due to charge injection in switched capacitor applications can be reduced. For the following investigation, the output voltage V_{OUT} is grounded in order to measure the leakage current I_L. The input voltage V_{IN} was swept from 0 V to 5 V, whereby the maximum leakage current occurs on the maximum voltage difference $V_{IN} - V_{OUT}$ across the switch. The resulting leakage current I_L over temperature is shown in Figure 5.3.

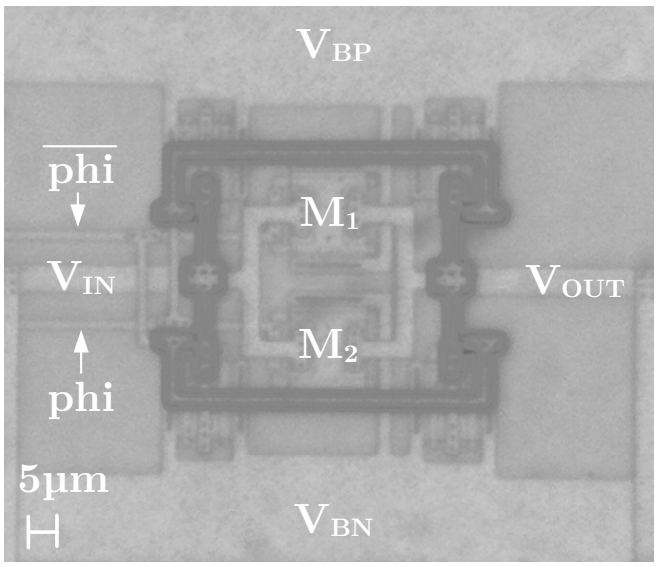

Figure 5.2: Chip photograph of the symmetrical analog switch in the considered SOI technology.

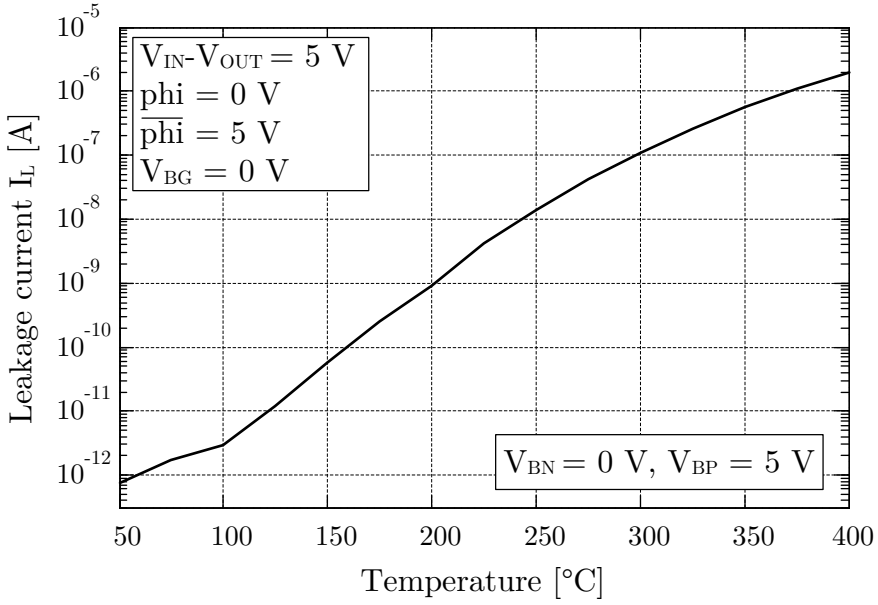

Figure 5.3: Experimental results of the leakage current I_L over temperature at the maximum of $V_{IN} - V_{OUT}$.

It can be seen that the leakage current increases dramatically with increasing temperature. At a temperature of 400 °C, the resulting off-state leakage current of the analyzed switch is reaching $I_L = 2\,\mu A$.

This leakage current leads to large errors in switched capacitor circuits [SKHK12]. The resulting error for the circuit depicted in Figure 5.4 a) is calculated as an example. For the calculation, a capacitor C_1 is assumed to be initially

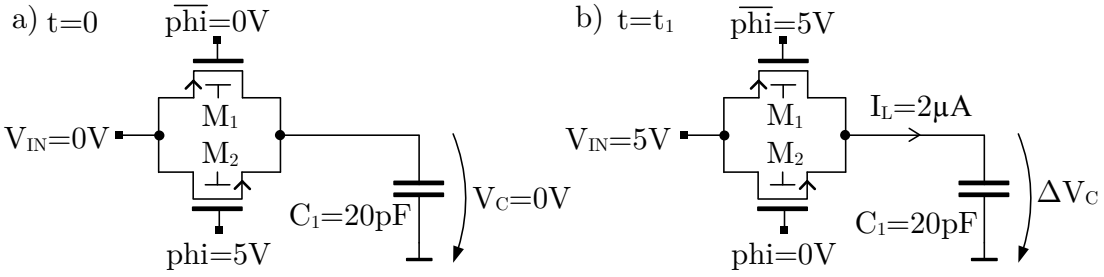

Figure 5.4: Example to demonstrate the resulting error due to leakage currents in analog switches. a) switch is turned on at $t = 0$. b) Switch is turned off at $t = t_1$.

discharged to 0 V, when the switch is turned on. For simplicity, charge injection and also charge injection compensation structures are neglected in this example.

The value of the storage capacitor C_1 is assumed to be 20 pF. At the time t_1, shown in Figure 5.4 b), the switch is turned off while the input voltage is set to $V_{IN} = 5\,\mathrm{V}$. The switch is closed for a period of time T, which represents one clock cycle. The period T is 10 µs for a clocking frequency of 100 kHz. The resulting error voltage at the storage capacitor C_1 after one clock period $\Delta t = T$ is then given by

$$\Delta V_C = \frac{\Delta Q}{C_1} = \frac{I_L \Delta t}{C_1} = \frac{2\,\mu\mathrm{A} \cdot 10\,\mu\mathrm{s}}{20\,\mathrm{pF}} = 1\,\mathrm{V}\ . \tag{5.1}$$

It might be obvious that an error of 1 V is not tolerable with a signal voltage range of 5 V. The minimization of leakage currents in analog switches is therefore necessary in order to maintain sufficient accuracy within switched capacitor circuits at high temperatures.

5.1.2 Current Mirrors

Current mirrors are widely used in various analog circuits, e.g. in operational amplifiers, operational transconductance amplifiers or voltage reference circuits. Errors in these current mirrors can be responsible for inaccuracies or even lead to malfunctions.

Basic N-channel and P-channel current mirrors are shown in Figures 5.5 a) and 5.5 b), respectively. All transistors have a channel width of 32 µm and a channel length of 12 µm in order to achieve a high output resistance. A chip photograph of both current mirrors is shown in Figure 5.6.

For the N-channel SOI-MOSFET current mirror in Figure 5.5 a), the input current I_1 is mirrored to the output current I_2. In case both devices match exactly

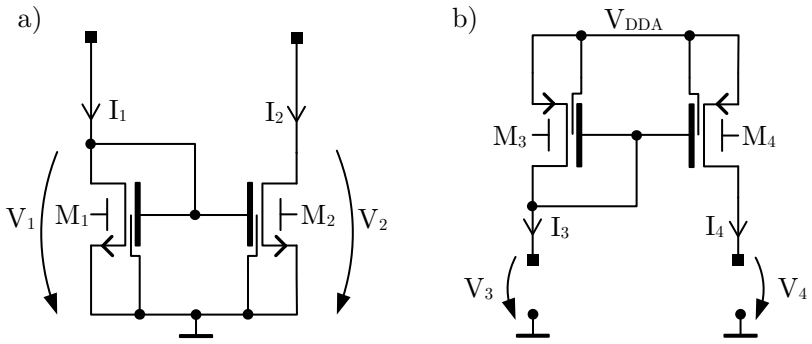

Figure 5.5: Basic current mirror of either a pair of a) N-channel SOI-MOSFETs and b) P-channel SOI-MOSFETs.

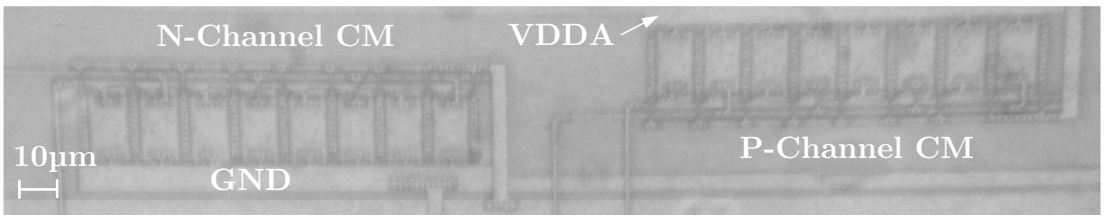

Figure 5.6: Chip photograph of an N-channel HGATE current mirror and a P-channel HGATE current mirror in the considered SOI technology.

in dimensions and threshold voltage, the difference $I_2 - I_1$ is affected by the channel length modulation effect. Since the gate and the drain of M_1 are short-circuited, V_1 is nearly equal to the threshold voltage of M_1. The use of current mirrors in high temperature applications is critical for very small currents in the range of the device leakage level. Precise current mirrors are therefore required, especially for applications where small currents need to be duplicated with a small error. One example is the use in precision bandgap voltage references, where small non-linear correction currents are used to eliminate the non-linear temperature dependence of the output voltage [Chr12]. The operation of the basic current mirror with very small currents is investigated in this section. The input current I_1 is 100 nA. The output current I_2 is investigated experimentally as a function of output voltage V_2 for different temperatures up to 400 °C and is shown in Figure 5.7 a). Figure 5.7 b) shows the resulting error $(I_2 - I_1)/I_1$ in percent over the output voltage V_2 for different temperatures.

It can be seen from Figure 5.7 b) that the resulting error is smaller than 4 % up to a temperature of 250 °C. This error can be considered as an systematical error since it is induced by channel length modulation rather than by leakage currents in case V_{DS1} and V_{DS2} are not equal.

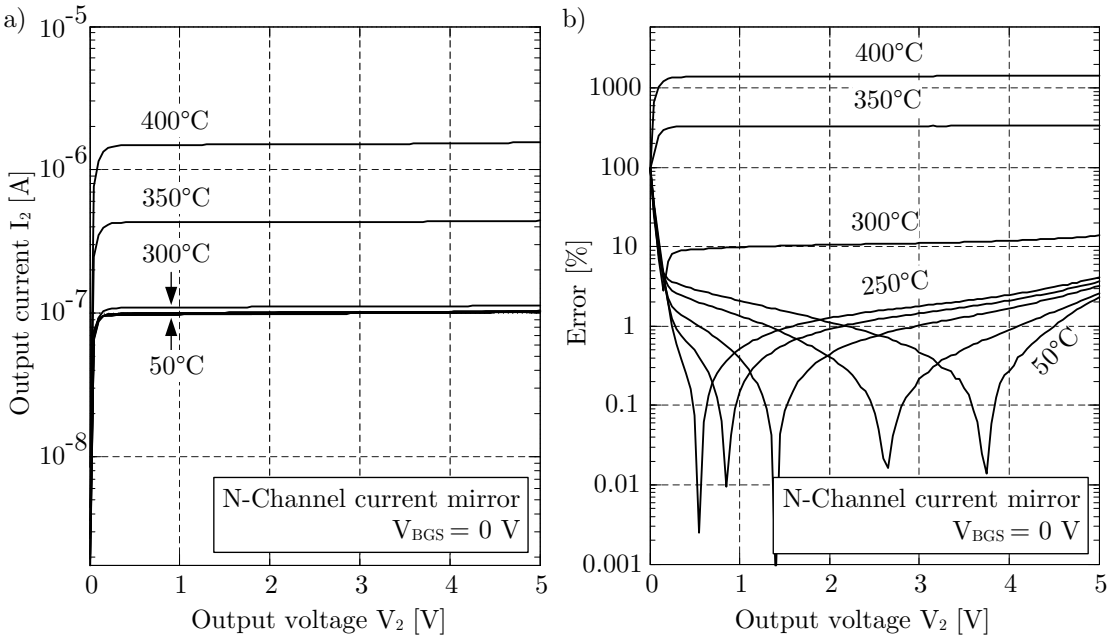

Figure 5.7: a) output current I_2 over output voltage V_2 of an N-channel current mirror for different temperatures. b) resulting error in percent over output voltage V_2 for different temperatures.

The error is given by Equation (5.2) in case the threshold voltage and (W/L) ratios of both transistors match [AH12].

$$\frac{I_2}{I_1} = \frac{1 + \lambda_1 V_{DS1}}{1 + \lambda_2 V_{DS2}} \tag{5.2}$$

Nevertheless, an increase of the overall error can be seen for temperatures above 250 °C. At 300 °C, the error is larger than 10 % and increases up to 1455 % at 400 °C. The error is caused by leakage currents, which are larger than the input current I_1 at high temperatures.

Measurement results of the output current I_4 over output voltage V_2 for the P-channel current mirror consisting of transistors M_3 and M_4 are shown in Figure 5.8 a). The measurements were carried out with an input current of $I_3 = 100\,\text{nA}$. Similar to the N-channel current mirror, the systematical error for this current mirror is less than 8 %. At a temperature of 350 °C, the maximum error increases up to 93.3 %. Due to very high leakage currents at 400 °C, the resulting error increases up to 455 %.

The presented results demonstrate how basic analog circuit components, like current mirrors are affected by leakage currents at very high temperatures. As a consequence, high errors for very low current applications up to 400 °C cannot be avoided with the standard approach. On the other hand, the increasing influence

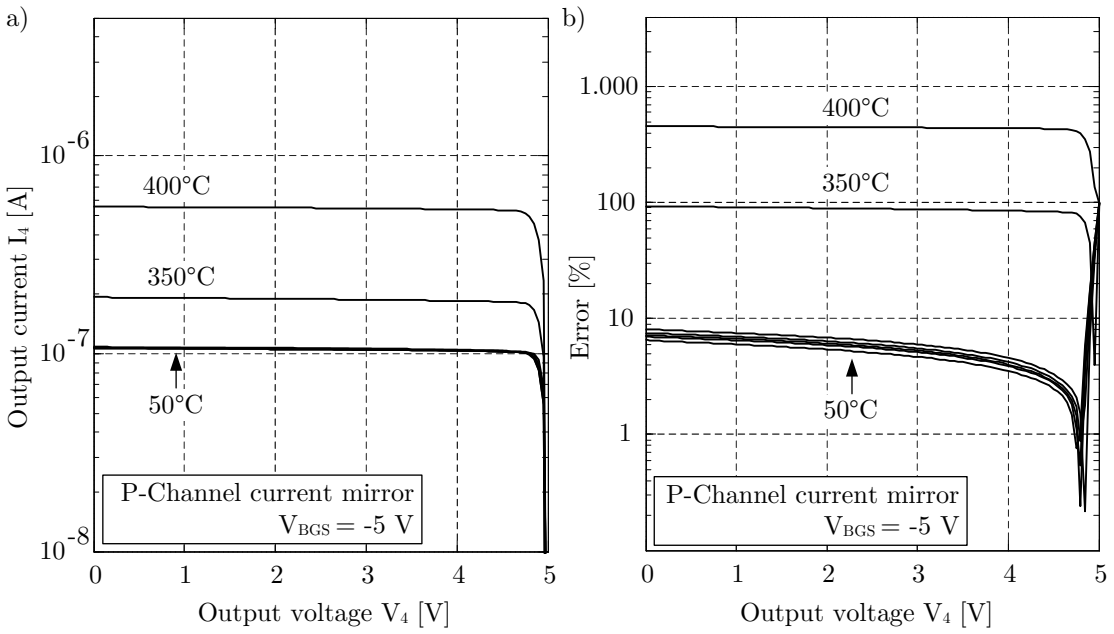

Figure 5.8: a) output current I_4 over output voltage V_4 of a basic P-channel current mirror for different temperatures. b) resulting error in percent over output voltage V_4 for different temperatures.

of leakage currents at high temperatures might not be noticed if these current mirrors are used to provide bias currents in the range of several micro amperes. Nevertheless, the reduction of leakage currents in SOI-MOSFET devices would also allow increased precision analog circuity at elevated temperatures.

5.1.3 Operational Amplifiers

Operational amplifiers are fundamental analog circuit building blocks required in a variety of different applications. They can be optimized, either to reach high open loop DC gains or high bandwidths. Whether the requirements are high DC gain or high bandwidth, the gain stages of the operational amplifier are typically biased in weak or strong inversion. As it was discussed before, the moderate inversion region offers a good trade-off between intrinsic gain and bandwidth [Bin07b]. Due to the fact that weak inversion requires very low current densities within the gain stages, this operating point is intensively affected by leakage currents of SOI-MOSFET devices. A safe biasing approach at very high temperatures is to bias the devices in strong inversion with sufficient margin to the leakage current level. In this case, operation of the amplifier can be maintained also at high temperatures. As a consequence, the resulting open loop DC gain of the op-amp is low compared to the values achieved weak inversion- or moderate inversion.

Since strong inversion is not critical due to high current densities, high bandwidth op-amps can easily be realized with high bias currents and small devices sizes. Nevertheless, high gain applications at high temperatures suffer from insufficient open loop DC gain [SKK11]. In the following analysis, the open loop DC gain of a simple two-stage operational amplifier with Miller compensation is investigated. A schematic view of the amplifier is shown in Figure 5.9 and a chip photograph is shown in Figure 5.10.

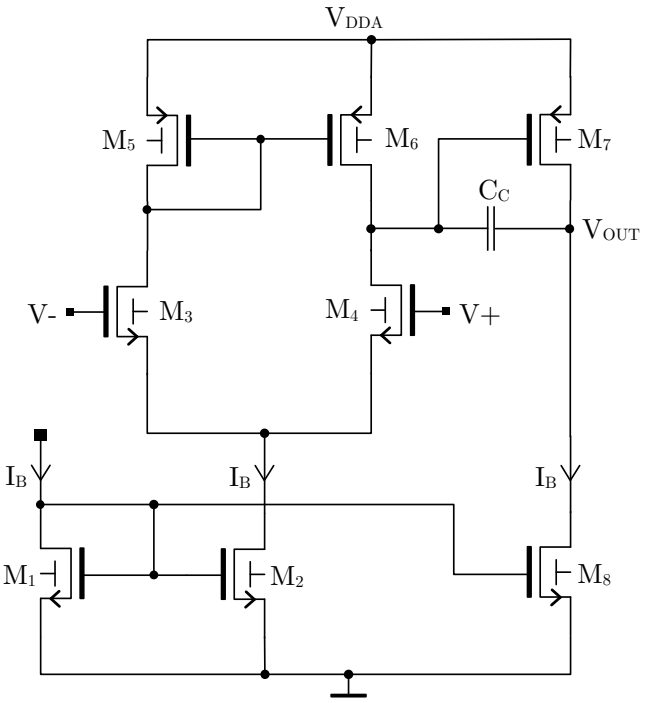

Figure 5.9: Schematic view of a two-stage operational amplifier with Miller compensation.

The total open loop DC gain A_0 of the operational amplifier is the product the open loop DC gain of both gain stages and is given in (5.3) [KB06].

$$A_0 = \left(\frac{g_m}{I_d}\right)_4 \left(\frac{g_m}{I_d}\right)_7 (V_{A4}||V_{A6})\,(V_{A7}||V_{A8}) \tag{5.3}$$

The bias current I_B is mirrored equally into the first and second gain stage. For a bias current of $I_B = 3.3\,\mu A$ and a W/L ratio of 16, the transistors M_3, M_4 and M_7 operate in the mid moderate inversion region. All channel lengths are $4.8\,\mu m$. All current mirror devices operate in strong inversion since high Early voltages are required for high output resistances. The open loop DC gain at an operating point of $V_{DDA}/2$ was measured as a function of temperature and is shown in Figure 5.11. Measurements were carried out at a frequency 10 Hz using

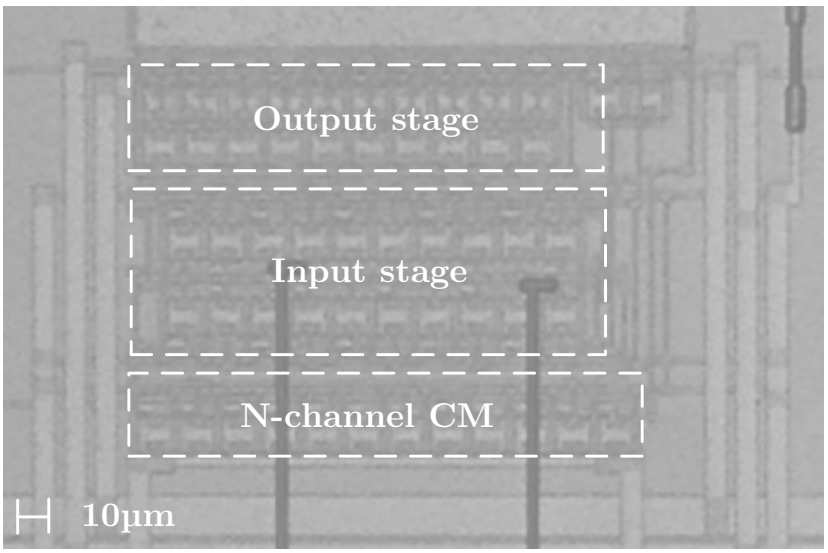

Figure 5.10: Chip photograph of the two-stage operational amplifier in the considered SOI technology.

a network analyzer and a DC offset of $V_{DDA}/2$ at the positive input node of the amplifier. The output of the amplifier was buffered using an external wideband J-FET amplifier to decouple the load of the network analyzer. The influence of the J-FET amplifier was eliminated by the calibration of the overall signal path. The entire measurement setup is described in detail in appendix A.4.

As one can see from these measurement results, the operational amplifier features an open loop DC gain of approximately 80 dB at low temperatures. The DC gain reduces starting from approximately 225 °C. Further increase of the operating temperature significantly reduces the open loop DC gain. The maximum operating temperature in moderate inversion is 275 °C.

These results demonstrate how operational amplifiers, working in moderate inversion for high gain applications, are affected by increasing operating temperatures.

5.1.4 Voltage References

A bandgap voltage reference circuit provides a reference voltage, which is in a first order approximation independent on supply voltage and temperature. At high temperatures, increased leakage currents, decreased threshold voltages and the loss of DC gain in implemented operational amplifiers lead to large errors in the output reference voltage. Measurement results of a regular bandgap reference up to 450 °C were demonstrated in [GDS+12], where a nonlinear increase of the

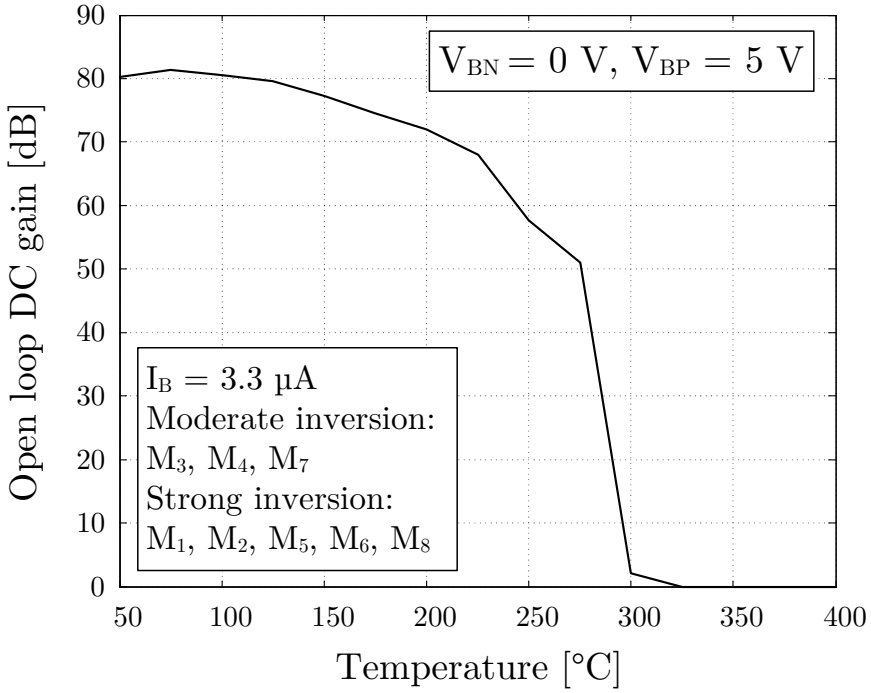

Figure 5.11: Experimental results of the DC open loop gain of the two-stage operational amplifier over temperature.

reference voltage above 250 °C was observed. A first order bandgap reference is investigated in this section. The schematic view of the first order bandgap voltage reference is shown in Figure 5.12. A photograph of the voltage reference in shown in Figure 5.13.

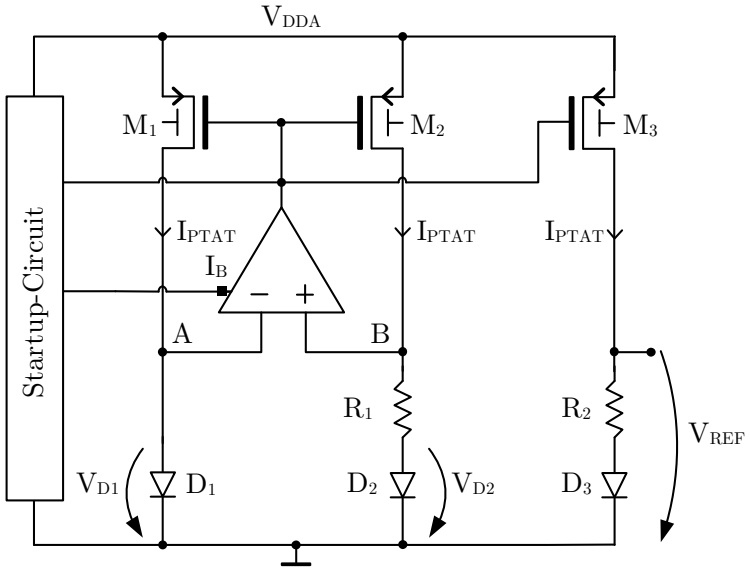

Figure 5.12: Schematic view of the first order bandgap voltage reference.

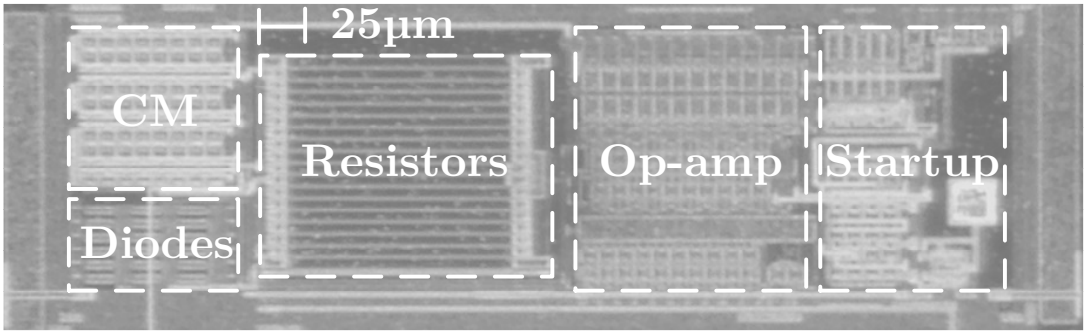

Figure 5.13: Photograph of the first order bandgap voltage reference in SOI technology.

PIN-diodes are utilized in the bandgap circuit to generate the PTAT (Proportional To Absolute Temperate) current I_{PTAT}. The two-stage Miller op-amp, which was investigated in the previous section, was used to control the voltage difference between the nodes A and B. In this application, the op-amp is usually biased and designed to reach high open loop DC gain values in order to minimize the voltage difference at these nodes. The diode area of D_2 is k times larger than the diode area of D_1 and D_3. Since the voltages at the nodes A and B are equal, the difference in diode voltages of D_2 and D_1 drops across R_1. The current I_{PTAT} in both bandgap core paths is then given by (5.4) [Chr12].

$$I_{PTAT} = \frac{V_{D1} - V_{D2}}{R_1} = \frac{V_t \cdot ln\,(k)}{R_1} \tag{5.4}$$

and the reference output voltage V_{REF} results in

$$V_{REF} = I_{PTAT} \cdot R_2 + V_{D3} = \frac{R_2}{R_1} V_t \cdot ln\,(k) + V_{D3}\ . \tag{5.5}$$

Measurement results of the reference output voltage V_{REF} up to 425 °C with a supply voltage of $V_{DDA} = 5\,\text{V}$ are shown in Figure 5.14. The reference voltage starts to increase rapidly from around 325 °C and reaches 2.8 V at 425 °C.

The reason for the increase in output voltage at high temperatures is the low threshold voltage of P-channel devices used in the current source devices M_1-M_3. It was shown in Figure 4.3 in Section 4.2, that the threshold voltage of P-channel devices without back gate effect is reduced to around $-0.5\,\text{V}$ at 400 °C. In the bandgap voltage reference, a back gate effect of $V_{BGS} = -5\,\text{V}$ further reduces the threshold voltage of P-channel devices. It is thereby expected that the threshold voltage of P-channel devices reaches 0 V at 400 °C. As a result, the op-amp operates near the positive supply voltage, and is limited by the output swing of the operational amplifier. This results in an increased I_{PTAT} current,

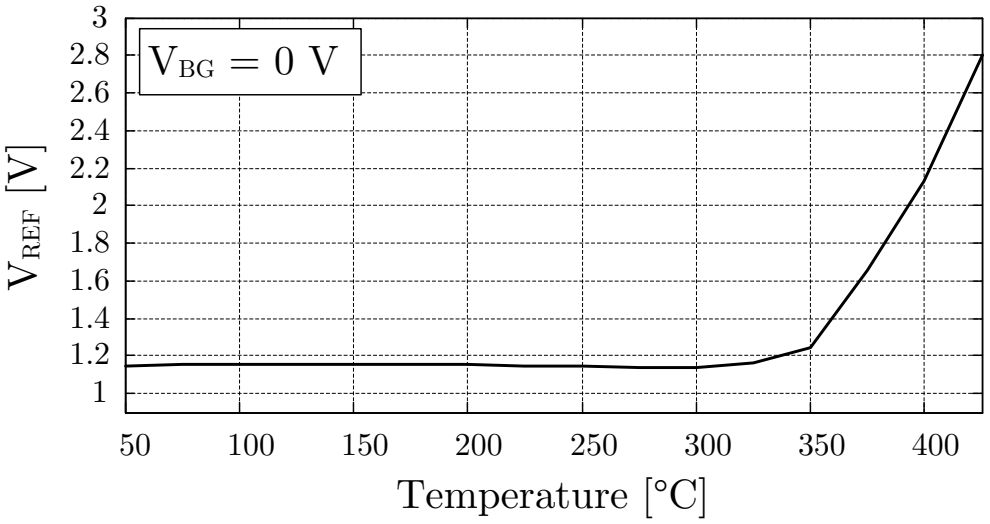

Figure 5.14: Measurement results of the bandgap reference voltage V_{REF} over temperature.

causing the increase of the output voltage V_{REF}. High threshold voltages can be used to avoid this error in case they are available in the considered SOI technology. Nonetheless, the operational amplifier has to operate properly up to 400 °C. Only strong inversion operation of the op-amp's gain stages is feasible, as discussed before. The low achievable overall open loop DC gain of the op-amp then further increases the error of the bandgap output voltage.

5.2 Summary

High temperature operation capabilities of basic analog circuits were demonstrated in this chapter. Analog switches, basic current mirrors and more complex analog building blocks like operational amplifiers and voltage references were investigated. They are significantly affected by increasing operating temperatures. Increased leakage currents in analog switches lead to significant errors in switched capacitor applications whereby switching speed and capacitor sizes cannot easily be increased without the loss of accuracy and increasing die area. The reduction of leakage currents in analog switches is therefore required in order to realize switched capacitor circuitry at very high temperatures.

It was also shown that basic current mirror topologies are affected by leakage currents in case they are operated with very small drain currents. Improved current mirrors with reduced subthreshold leakage currents are required for applications, where these small operating currents are used. The influence of

leakage currents on these basic current mirrors might be low in case they are used to bias circuit blocks in the range of several micro amperes.

In case ambient temperatures up to 400 °C are targeted, the operating point of operational amplifiers is limited to strong inversion for all devices inside the operational amplifier. Otherwise leakage currents tend to decrease the intrinsic gain of the amplifier stages, which results in a sudden drop of open loop DC gain at high temperatures. While strong inversion remains as the only possible operating point at high temperatures, the maximum achievable open loop DC gain of the amplifier is low compared to operation in moderate inversion.

Bandgap voltage references are also affected by the increase in temperature. The decreased threshold voltage of P-channel SOI-MOSFETs at very high temperatures has the most significant effect on the output voltage of the reference circuit. Additional sources of errors exist since also current mirrors and an operational amplifier are used.

The circuits investigated in this chapter are significantly affected by device leakage currents and decreased threshold voltage at high temperatures. A reduction of the subthreshold leakage current and an increase of threshold voltage at high temperatures are expected to reduce these errors and might allow circuit operation up to 400 °C. In the following chapter, it will be investigated, how reverse body biasing can be used in order to solve these issues.

Chapter 6

Improved SOI-MOSFET Characteristics at High Temperatures

It was shown in the preceding chapters, how high temperatures affect the analog characteristics of SOI-MOSFETs as well as the operation of analog circuits. In this chapter, the effect of reverse body biasing (RBB) on SOI-MOSFET device characteristics is investigated. Reverse body biasing was found useful in influencing the threshold voltage and the breakdown characteristics of SOI-MOSFET devices. It is also known for the reduction of off-state leakage currents in digital circuits [MHY+99]. However, there are no known sources of research work targeting the effect of RBB on analog SOI-MOSFET device characteristics, e.g. the g_m/I_d factor, intrinsic gain and intrinsic bandwidth, at high temperatures.

6.1 Reverse Body Biasing (RBB)

Body biasing refers to the biasing of the film (body) region of the SOI-MOSFET with a voltage, which is different to the source voltage of the device. In SOI technology, body biasing can only be realized with body-contacted devices, such as HGATE devices. For example, the body of an N-channel HGATE SOI-MOSFET device can be biased in forward direction ($V_{BS} > 0$), referred to as forward body biasing (FBB) and in reverse direction ($V_{BS} < 0$), referred to as reverse body biasing (RBB).

In non-biased devices, as in Split-Source SOI-MOSFETs in the considered technology, the body-source PN-junction is short-circuited. In general, reverse body biasing is realized by biasing the body-source PN-junction in negative

(reverse) direction. Since in most cases, the source of N-channel SOI-MOSFETs is connected to ground potential, reverse biasing of N-channel devices is achieved by biasing the body of the device lower than ground potential. For P-channel SOI-MOSFETs, reverse biasing can be realized if the body of the device is biased with a voltage higher than the source potential of the device. In most cases, the source of P-channel SOI-MOSFETs is connected to the positive supply voltage. The body potential therefore has to be higher than the positive supply voltage in order to achieve RBB for P-channel devices. The biasing voltages of both, N-channel and P-channel SOI-MOSFETs are shown in Figure 6.1.

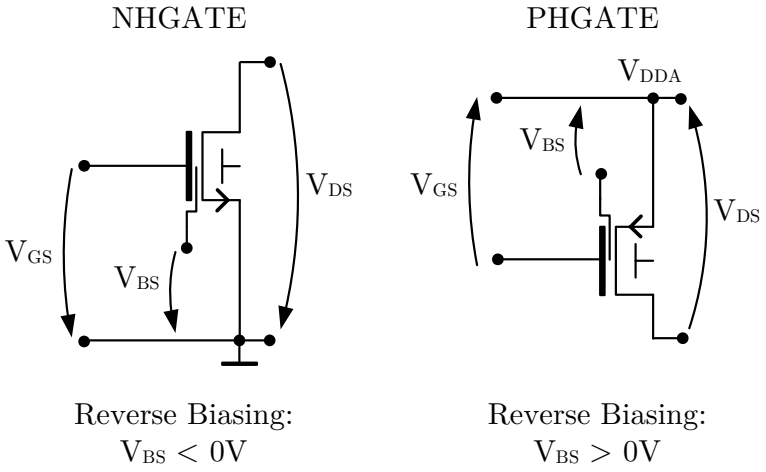

Figure 6.1: Reverse body biasing (RBB) of N-channel and P-channel SOI-MOSFETs.

As it can be seen from this figure, reverse body biasing of N-channel SOI-MOSFETs is achieved with a body-source voltage of $V_{BS} < 0V$. For P-channel SOI-MOSFETs, reverse bias is realized with a body-source voltage of $V_{BS} > 0V$. In the following sections, the influence of RBB on the analog SOI-MOSFET device characteristics at high temperatures is discussed in detail.

6.2 Depletion State of the Silicon Film

It was shown in Section 3.7 that the front gate depletion depth x_{d1} is influenced by the potential difference across the front gate surface potential and the film potential V_B. In case a body-source voltage of $V_{BS} \neq 0$ is considered, its influence on the depletion depth x_{d1} can be written as in Equation (6.1).

$$x_{d1}\left(V_{BS}\right) = \sqrt{\frac{2\epsilon_{si}\left(\phi_{S1} - V_{BS}\right)}{qN_{CH}}} \tag{6.1}$$

In case a front gate-source voltage of $V_{GS1} = 0\,\mathrm{V}$ is applied to a partially depleted N-channel SOI-MOSFET, the front gate surface potential ϕ_{S1}, which was given in Equation (3.25) in Section 3.2, is mainly determined by the flatband voltage V_{FB1} and thereby by the metal-semiconductor work function difference ϕ_{ms1}.

One can see from Equation (6.1) that the depletion depth x_{d1} increases with increasing reverse bias. In case a sufficient negative reverse body bias is applied to the film, the depletion depth x_{d1} is extended to reach the back interface of the device. Like the front gate depletion depth x_{d1}, also the back gate depletion depth x_{d2} extends further into the silicon film. The back gate depletion depth can be neglected here, since it is significantly smaller than the front gate depletion depth. Nevertheless, a thin depletion depth will remain at the back gate interface. The depletion depth x_{d1} over channel doping concentration and temperature with a gate-source voltage of $V_{GS1} = 0\,\mathrm{V}$ is shown in Figures 6.2 a) and 6.2 b) for $V_{BS} = 0\,\mathrm{V}$ and $V_{BS} = -0.4\,\mathrm{V}$, respectively. The film thickness t_{SI} is 150 nm.

With a channel doping concentration of $N_{CH} = 1.3 \cdot 10^{16}\,\mathrm{cm}^{-3}$, the front gate depletion depth starts to decrease from around 100 °C. Below that temperature, the silicon film of the SOI-MOSFET device is fully depleted. Above 100 °C, the depletion depth x_{d1} is smaller than the film thickness and the device becomes partially depleted. With an applied RBB of $V_{BS} = -0.4\,\mathrm{V}$ for a channel doping concentration of $N_{CH} = 1.3 \cdot 10^{16}\,\mathrm{cm}^{-3}$, as shown in Figure 6.2 b), the depletion depth x_{d1} does not change with temperature. As a, the film of the SOI-MOSFET device with applied RBB remains fully depleted also at high temperatures.

As a major result, it can be concluded that a partially depleted SOI-MOSFET can be turned into a fully depleted SOI-MOSFET, when sufficient RBB is applied to the device. In the considered SOI technology, a RBB voltage of $V_{BS} = -1\,\mathrm{V}$ is sufficient to achieve fully depleted N-channel and P-channel devices up to a temperature of 400 °C. The minimum reverse bias voltage as well as the influence of applied reverse body biasing on the front gate surface potential is investigated in the following sections.

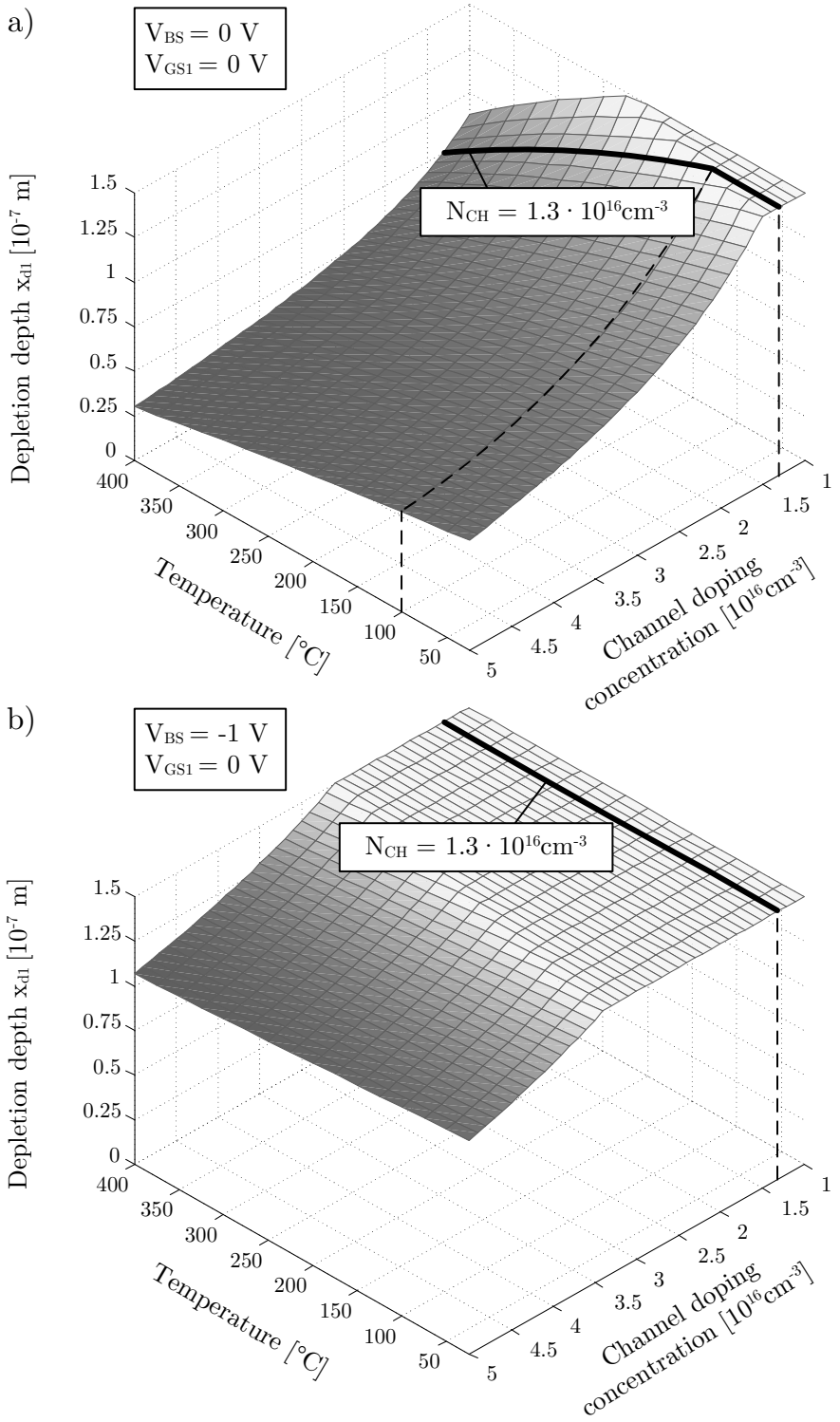

Figure 6.2: a) depletion depth x_{d1} over channel doping concentration and temperature without RBB ($V_{BS} = 0\,\mathrm{V}$). b) depletion depth x_{d1} over channel doping concentration and temperature with RBB ($V_{BS} = -0.4\,\mathrm{V}$).

6.3 Minimum Reverse Bias Voltage

The feasibility of RBB in different SOI technologies can be estimated by the calculation of the minimum reverse bias voltage V_{BSmin}. For a fully depleted SOI-MOSFET the front gate depletion depth x_{d1} extends to the back interface of the silicon film and is then equal to t_{SI} if the back gate effect is neglected.

$$x_{d1}(T) = \sqrt{\frac{2\epsilon_{si}(\phi_{S1} - V_{BS})}{qN_{CH}}} \stackrel{!}{=} t_{SI} \tag{6.2}$$

Solving Equation (6.2) for V_{BS} yields the minimum reverse bias voltage V_{BSmin} as shown in Equation (6.3).

$$V_{BSmin}(T) = \phi_{S1} - \frac{qN_{CH}t_{SI}^2}{2\epsilon_{si}} \tag{6.3}$$

In PD mode, the front gate surface potential ϕ_{S1} can be calculated using Equation (3.25), which was given in Section 3.2.1. As a requirement, the device should also be fully depleted if the minimum reverse bias is applied with a gate-source voltage of $V_{GS1} = 0\,\mathrm{V}$. Therefore, the front gate-source voltage V_{GS1} in (3.25) is set to zero. Equation (6.3) in combination with Equations (3.25) and (3.18) then yields

$$V_{BSmin}(T) = \left[-\frac{\gamma_1}{2} + \sqrt{\left(\frac{\gamma_1}{2}\right)^2 - \phi_{ms1}(T)}\right]^2 - \frac{qN_{CH}t_{SI}^2}{2\epsilon_{si}} \tag{6.4}$$

with the body effect coefficient γ_1 given by

$$\gamma_1 = \frac{\sqrt{2q\epsilon_{si}N_{CH}}}{C'_{OX1}}. \tag{6.5}$$

In Equation (6.4), the metal-semiconductor work function difference $\phi_{ms1}(T)$ is the only temperature dependent factor. It was introduced by Equation (3.19) in Section 3.2.1 and is given again for convenience in Equation (6.6) [SN07].

$$\phi_{ms1} = \phi_m - \phi_s = \phi_m - \left[\chi_{SI} + \frac{E_G(T)}{2q} + \phi_F\right] \tag{6.6}$$

The electron affinity of silicon is $\chi_{SI} = 4.05\,\mathrm{V}$ and ϕ_m is the work function of the poly-silicon gate, which is equal to 4.3 V. The Fermi potential for a p-type semiconductor is given by [SN07]

$$\phi_{Fp} \approx V_t \cdot ln\left(\frac{N_{CH}}{n_i}\right) \tag{6.7}$$

and the bandgap energy of silicon $E_G(T)$ can be written as [Col98]

$$E_G(T) = 1.17\,\text{eV} - \frac{4.73\,\text{eV/K} \cdot 10^{-4} \cdot T^2}{T + 636\,\text{K}}. \tag{6.8}$$

Finally, the intrinsic carrier concentration in silicon n_i can be written as [Col98]

$$n_i = 3.9 \cdot 10^{16} \cdot T^{3/2} \cdot exp\left(\frac{-E_G(0)}{2kT}\right). \tag{6.9}$$

The required minimum reverse bias voltage for a fully depleted silicon film is a function of doping concentration N_{CH}, front gate oxide thickness t_{OX1}, metal-semiconductor work function difference ϕ_{ms1} and silicon film thickness t_{SI}.

$$V_{BSmin} = f(N_{CH}, t_{OX1}, \phi_{ms1}, t_{SI}) \tag{6.10}$$

The required reverse bias V_{BSmin} for a temperature of $T = 400\,°\text{C}$ was calculated for different film thicknesses and doping concentrations and is shown in Figure 6.3.

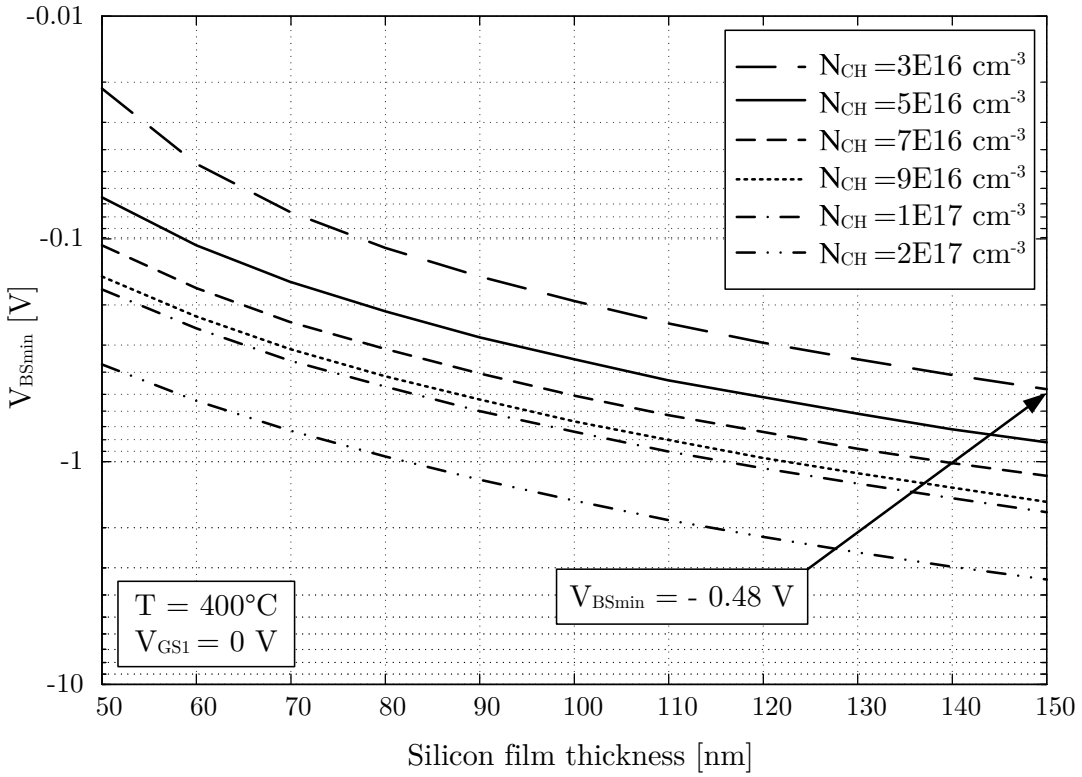

Figure 6.3: Calculated minimum reverse bias voltage V_{BSmin} at 400 °C calculated from (6.3).

It can be seen from Figure 6.3 that a reverse bias voltage of $V_{BSmin} = -0.48\,\text{V}$ is required for a silicon thickness of 150 nm and for example a doping concentration

of $N_{CH} = 3 \cdot 10^{16}\,\mathrm{cm}^{-3}$. In case of smaller technology nodes, a higher doping concentration has to be used to maintain the same threshold voltage. In case smaller technology node are used with the same film thickness and a doping concentration of $N_{CH} = 1 \cdot 10^{17}\,\mathrm{cm}^{-3}$, the required minimum reverse bias voltage increases to approximately $V_{BSmin} = -1.7\,\mathrm{V}$. On the other hand, V_{BSmin} is reduced if the film thickness is reduced. It it important to mention here that these results were obtained for a specific metal-semiconductor work function difference, which was calculated using Equation (6.6). This has to be considered when calculating the minimum required reverse bias voltage for other SOI technologies.

6.4 Surface Potentials

It was shown in the previous section that the depletion state of the SOI-MOSFETs can be influenced by applying RBB. Thereby, N-channel and P-channel SOI-MOSFET turn from partially depleted to fully depleted when RBB is applied. In case the device is biased with V_{BSmin} (400 °C), the devices remain fully depleted up to 400 °C.

Due to the transition from partially depleted to fully depleted, the front gate surface potential and the back gate surface potential in fully depleted mode cannot be considered independent from each other [Col04].

Expressions for both surface potentials were discussed in Section 3.2.2 and are again written in Equations (6.11) and (6.12).

$$\phi_{S1}|_{FD} = \left(1 + \frac{C_{si}}{C_{OX1}}\right)^{-1} \left[V_{G1} - \phi_{ms1} + \phi_{S2}\frac{C_{si}}{C_{OX1}} + \frac{Q'_d}{2C'_{ox1}}\right] \tag{6.11}$$

$$\phi_{S2}|_{FD} = \left(1 + \frac{C_{si}}{C_{OX2}}\right)^{-1} \left[V_{G2} - \phi_{ms2} + \phi_{S1}\frac{C_{si}}{C_{OX2}} + \frac{Q'_d}{2C'_{ox2}}\right] \tag{6.12}$$

A change in the surface potential ϕ_{S2} results in a change of the surface potential ϕ_{S1}, as one can see from Equation (6.11). The relationship can be calculated from Equation (6.11) and is given by

$$\Delta\,\phi_{S1}|_{FD} = \left(1 + \frac{C_{si}}{C_{OX1}}\right)^{-1} \frac{C_{si}}{C_{OX1}}\Delta\phi_{S2} = \frac{C_{si}}{C_{si} + C_{OX1}}\Delta\phi_{S2} \approx 0.45\,\Delta\phi_{S2} \tag{6.13}$$

For the calculation in (6.13), the film capacitance is given by $C_{si} = (WL)\epsilon_{si}/t_{SI}$ and the front gate oxide capacitance is given by $C_{OX1} = (WL)\epsilon_{ox}/t_{OX1}$.

Figure 6.4 shows two calculated potential distributions for a temperature of 150 °C.

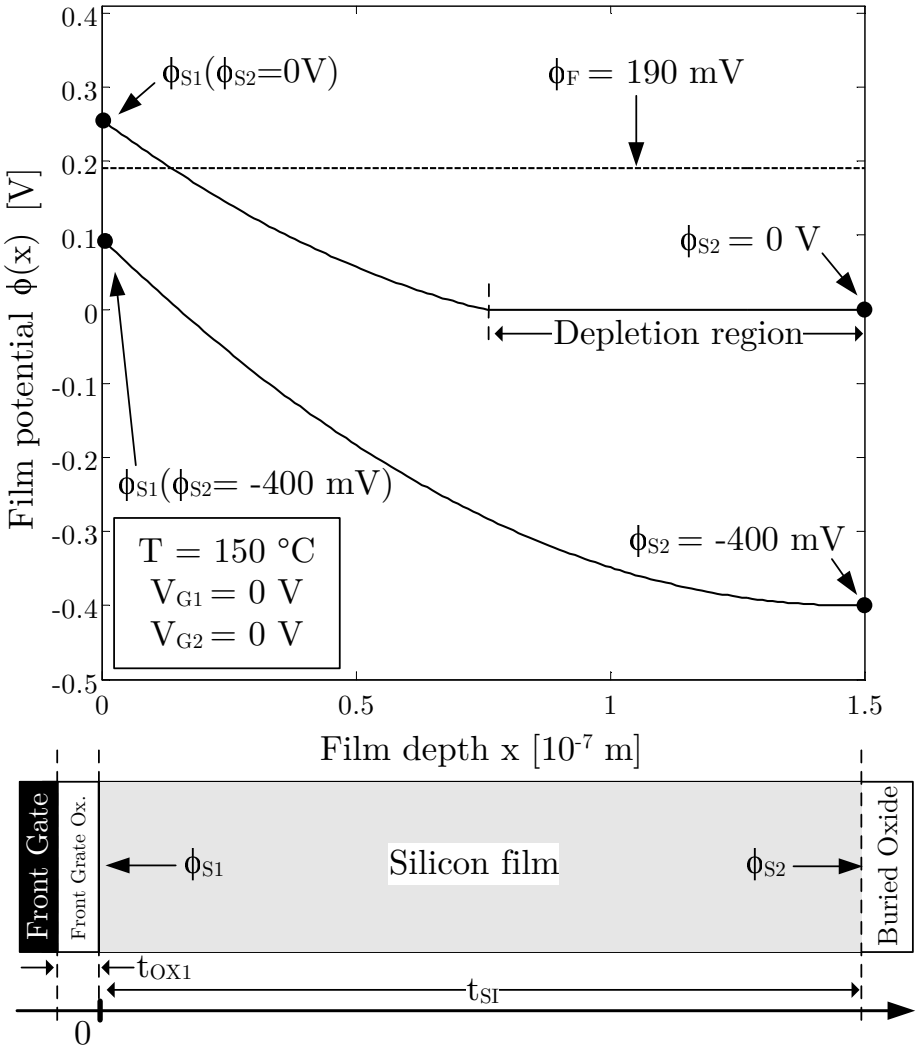

Figure 6.4: Calculated qualitative potential distribution $\phi(x)$ over silicon film depth x with a front- and back gate voltage of 0 V at a temperature of 150 °C.

The upper curve shows the calculated potential distribution $\phi(x)$ across the silicon film without applied RBB. The front surface potential ϕ_{S1} and back gate surface potential ϕ_{S2} were calculated using Equation (3.25). The potential distribution $\phi\,(x)$ was calculated using expression (6.14), which was adapted from Equation (3.37) given in Section 3.2.2.

$$\phi(x) = min\left[V_{BS}, \frac{qN_{CH}}{2\epsilon_{si}}x^2 + \left(\frac{\phi_{S2} - \phi_{S1}}{t_{SI}} - \frac{qN_{CH}t_{SI}}{2\epsilon_{si}}\right)x + \phi_{S1}\right] \tag{6.14}$$

The device is partially depleted as the potential decreases to 0 V in the middle of the film. The depletion depth x_{d2} at a temperature of 150 °C is small compared to the front gate depletion depth x_{d1} and is not visible in this illustration . Since the device is partially depleted, the front gate surface potential ϕ_{S1} is only determined by the flatband voltage V_{FB1}, the front gate voltage V_{G1} and the depletion charge. The depletion depth x_{d1} is approximately 75 nm. With the front gate voltage considered to be 0 V, the front gate surface potential is higher than the Fermi potential ϕ_F, which results in the front channel being in weak inversion. This effect was also observed from the weak inversion input characteristics from Figure 4.4 in Section 4.3. In case a reverse body bias is applied to the partially depleted device, the device turns fully depleted due to the increased potential difference across the front gate depletion region. In this case, the front gate potential and the back gate potential are coupled. The potential distribution across the silicon film of a fully depleted device is shown by the lower curve in Figure 6.4. In case the back gate surface potential ϕ_{S2} is reduced to −400 mV, the font gate surface potential ϕ_{S1} is reduced to approximately −150 mV due to the coupling of both potentials in fully depleted mode.

Whether the back gate surface potential ϕ_{S2} can be effectively controlled by an applied body potential in fully depleted mode was analyzed using *Synopsys Sentaurus (TCAD)*[1] 2D simulation results. Low temperatures are chosen for the simulation in order to investigate the effect of applied RBB on the back gate potential with a fully depleted silicon film. Table 6.1 lists all doping concentrations used for the TCAD simulation.

Table 6.1: Doping concentrations used for TCAD simulation.

Symbol	Description	Value	Unit
N_{CH}	Uniform film P^- doping concentration	$3 \cdot 10^{16}$	cm^{-3}
N_{Sub}	Uniform substrate (back gate) N^- doping concentration	$1 \cdot 10^{14}$	cm^{-3}
N_G	Uniform front gate N^+ doping concentration	$1 \cdot 10^{18}$	cm^{-3}
N_{BC}	Body contact P^+ doping concentration (peak)	$2 \cdot 10^{19}$	cm^{-3}

[1] *Sentaurus* is a registered trademark of Synopsys, Inc.

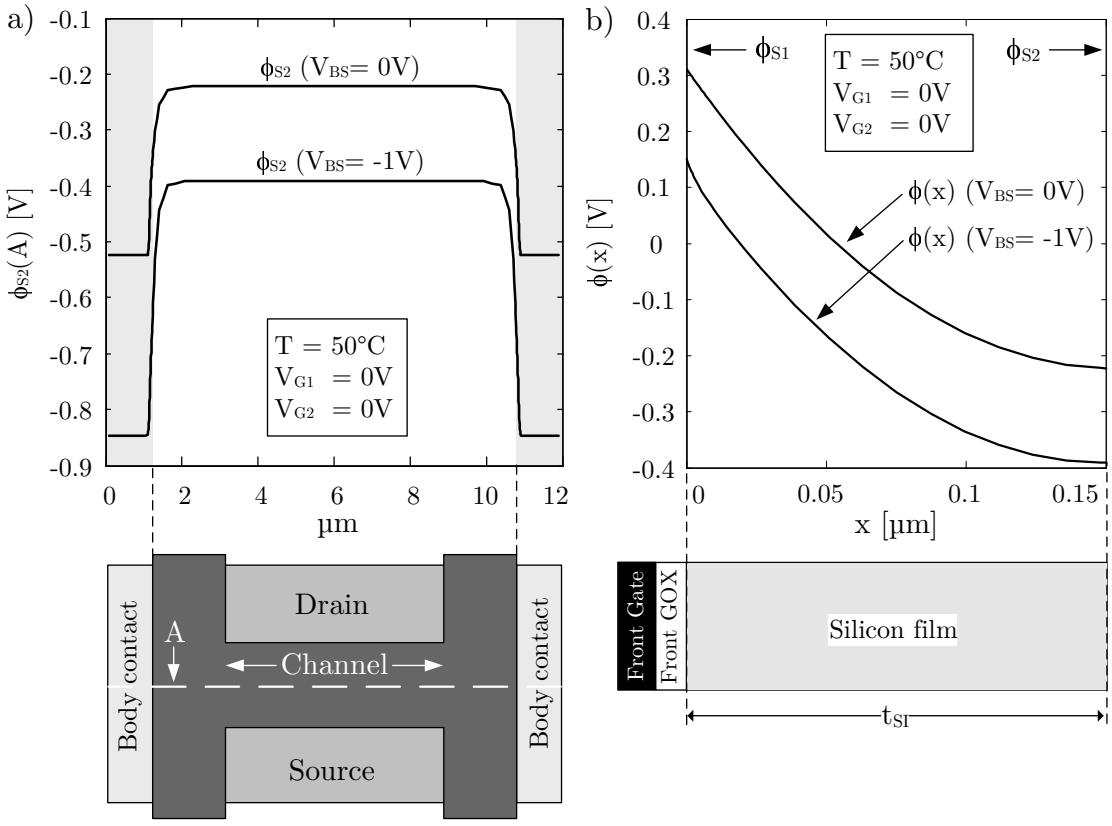

Figure 6.5: TCAD simulation results of surface potentials for an N-channel HGATE SOI-MOSFET at 50 °C. a) back gate surface potential ϕ_{S2} at cross section A with $V_{BS} = -1\,\mathrm{V}$ and without $V_{BS} = 0\,\mathrm{V}$ applied back bias. b) potential distribution across the silicon film in the center of the device.

The doping concentrations for gate, silicon film and substrate are uniformly distributed. A Gauss distribution was used for the doping concentration of the body contacts. Figure 6.5 a) shows the back gate surface potential ϕ_{S2} at the cross section A in the middle of the device channel. Source and drain regions were neglected in the 2D simulation. The simulation temperature is 50 °C and the device is fully depleted. It can be seen that an applied RBB voltage of $V_{BS} = -1\,\mathrm{V}$ at the body contact reduces the back gate potential across the silicon film by approximately 180 mV. The back gate potential of a fully depleted SOI-MOSFET can thereby be controlled by the applied body potential. This effect has also been reported by [MHY+99]. Figure 6.5 b) shows the potential distribution across the silicon film depth x in the center of the device in the middle of the channel. It can be seen here that the front gate surface potential ϕ_{S1} and the back gate surface potential ϕ_{S2} are coupled, as it was expected by the theoretical consideration.

A change in back gate surface potential thereby result is a change in front gate surface potential.

With the influence of the back gate surface potential, the front gate surface potential ϕ_{S1} decreases and is then lower than the Fermi potential ϕ_F. Thus, the front channel of the device is depleted and is not entering weak inversion with increasing temperature. As a result, the inversion state of the SOI-MOSFET channel is more effectively controlled by the gate-source voltage rather than by temperature, as it is the case in non-biased devices. The qualitative Fermi potential ϕ_F, calculated using Equation (3.12), and the front gate surface potential ϕ_{S1}, calculated using Equation (3.34), for a front- and back gate voltage of 0 V are shown over temperature in Figure 6.6.

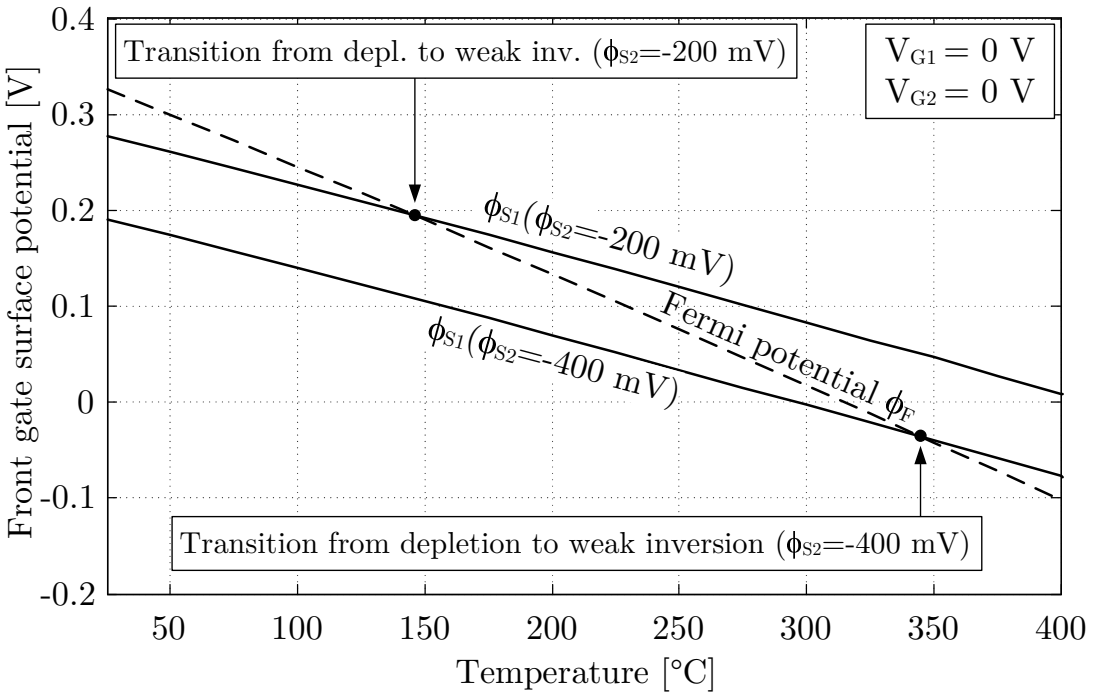

Figure 6.6: Qualitative Fermi potential and front gate surface potential ϕ_{S1} over temperature for a back gate surface potential of $\phi_{S2} = -200\,\text{mV}$ and $\phi_{S2} = -400\,\text{mV}$.

The front gate surface potential was plotted for back gate surface potentials of $-200\,\text{mV}$ and $-400\,\text{mV}$. It can be seen that the transition temperature, at which the front channel state changes from depletion to weak inversion, is shifting from approximately 150 °C ($\phi_{S2} = -200\,\text{mV}$) to approximately 350 °C ($\phi_{S2} = -400\,\text{mV}$). In this case, the front gate channel of the SOI-MOSFET device is effectively kept in depletion up to 350 °C, which has a significant effect on channel

leakage current as we will see in the later sections. The drain current of an N-channel SOI-MOSFET was measured as a function of gate-source voltage V_{GS} and is shown in Figures 6.7 a) and b) without and with applied RBB, respectively.

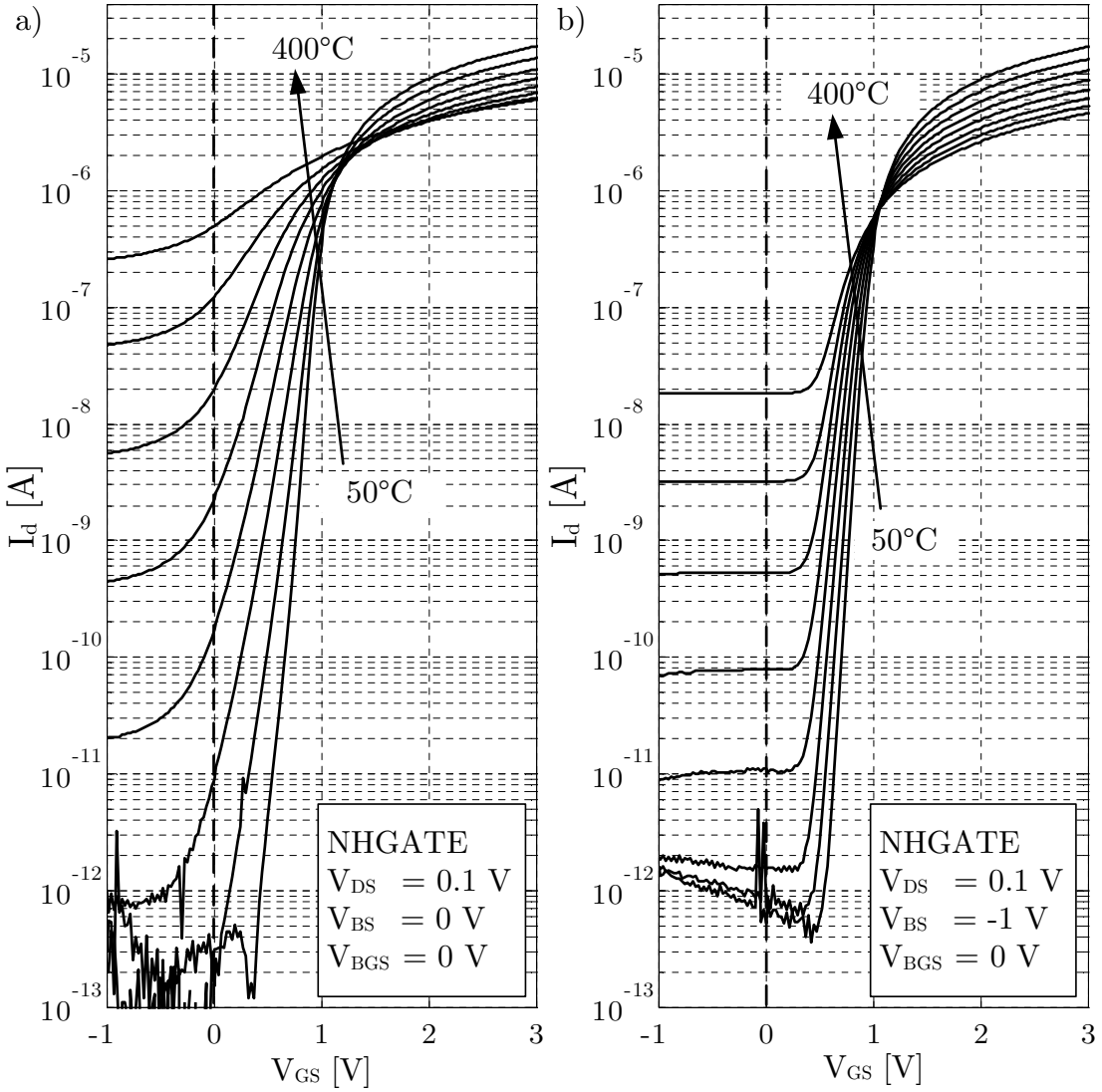

Figure 6.7: Weak inversion drain current of an N-channel SOI-MOSFET as a function of gate-source voltage V_{GS} for different temperatures from 50 °C up to 400 °C a) without RBB ($V_{BS} = 0\,\mathrm{V}$). b) with applied RBB ($V_{BS} = -1\,\mathrm{V}$).

In case the front gate interface of the N-channel SOI-MOSFET is in depletion state, it is expected that the drain current is not affected by a small increase in gate-source voltage. Otherwise, if the front gate interface is in weak inversion, the drain current is a strong function of the gate-source voltage.

It can be seen from Figure 6.7 a) that the slope of the drain current at $V_{GS} = 0\,\mathrm{V}$ is not zero, which results in the device being in weak inversion. When RBB

is applied, as shown in Figure 6.7 b), the slope of the drain current at $V_{GS} = 0\,\mathrm{V}$ is zero. A body bias of $V_{BS} = -1\,\mathrm{V}$ was applied to the N-channel SOI-MOSFET. Thus, the drain current is not visibly affected by small changes in gate-source voltage V_{GS} and the front gate is in depletion.

6.5 Body Factor

The body factor n of partially depleted and fully depleted SOI-MOSFETs was already discussed in Section 3.3. For fully depleted SOI-MOSFETs in the considered SOI technology, n is in the range of 1.09 and significantly larger in case the device is partially depleted. In weak inversion, n can be obtained from the subthreshold swing, which is given by

$$S = \frac{dV_{GS}}{d\,(logI_d)} = V_t \cdot n \cdot ln\,(10)\ . \tag{6.15}$$

Solving Equation (6.15) for the body factor n yields

$$n = \frac{S}{V_t \cdot ln\,(10)} = \left(\frac{dlog(I_d)}{dV_{GS}} V_t \cdot ln\,(10)\right)^{-1}\ . \tag{6.16}$$

The body factor n was investigated experimentally with and without applied RBB. It was extracted from the weak inversion input characteristics, which were shown in Figure 6.7, for different body-source voltages and with a gate-source voltage of $V_{GS} = 0.7\,\mathrm{V}$ and a drain-source voltage of $V_{DS} = 3\,\mathrm{V}$. A higher drain-source voltage was determined for this measurement, since the subthreshold leakage current reaches higher values for a drain-source voltage of $V_{DS} \gg V_t$. The resulting body factor is shown in Figure 6.8.

Without RBB, the body factor n increases significantly at high temperatures. This increase is due to the reduced depletion depth x_{d1} within the SOI-MOSFET device. The body factor decreases also at low temperatures when RBB is applied to the devices. It seems to be the case that n slightly increases also with applied RBB at high temperature. It should be mentioned here that with increasing temperature and a constant V_{GS} bias voltage, the inversion state of the device is changing from weak inversion to moderate inversion or even strong inversion. The increased value of n can be related to the change in inversion state. If the reverse body bias is decreased to $V_{BS} = -1\,\mathrm{V}$, the increase of n with temperature is reduced. However, the change in body factor with an applied RBB of $V_{BS} = -1\,\mathrm{V}$ is small compared to the non-biased condition.

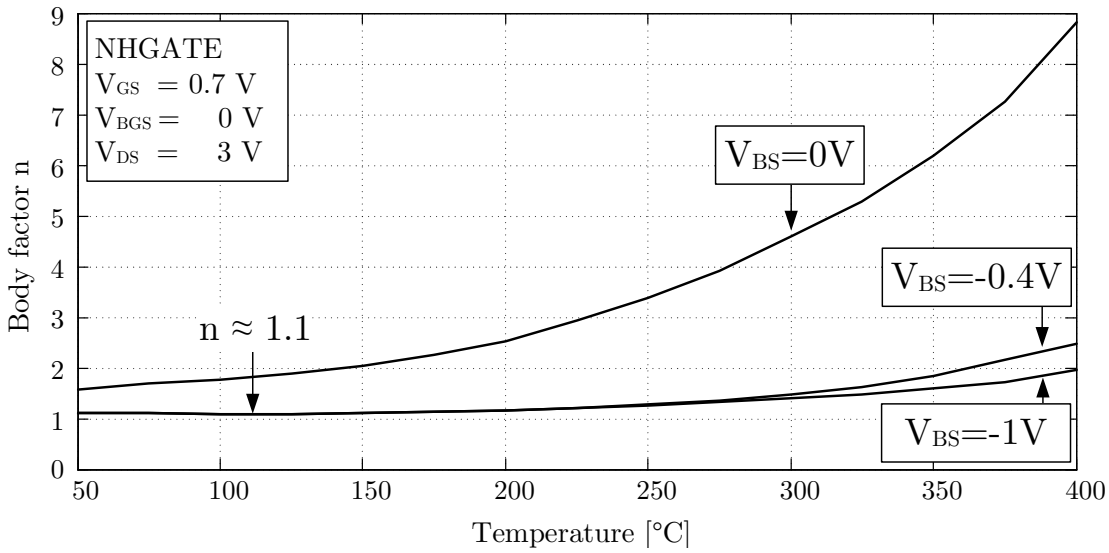

Figure 6.8: Body factor n of an N-channel SOI-MOSFET measured as a function of temperature with a gate-source voltage of $V_{GS} = 0.7\,\mathrm{V}$, a drain-source voltage of $V_{DS} = 3\,\mathrm{V}$ and a back gate-source voltage of $V_{BGS} = 0\,\mathrm{V}$ with and without applied RBB.

6.6 Threshold Voltage

With the change of the depletion state of the SOI-MOSFET's silicon film, there is also an expected change in threshold voltage, as the depletion charge in the film region beneath the gate is varied. The depletion depth is reduced when temperature increases. The depletion charge and threshold voltage of SOI-MOSFETs are thereby decreased. The temperature behavior of the threshold voltages of partially depleted and fully depleted SOI-MOSFETs were discussed in Section 3.6. Since a significant change in the depletion state was observed by applying RBB to the device, an influence on the threshold voltage is expected and investigated in detail in this section.

The threshold voltage of a partially depleted N-channel SOI-MOSFET with the influence of V_{BS} can be written as [Col04]

$$\begin{aligned} V_{thPD} &= \phi_{ms1} + 2\phi_F + \frac{qN_{CH}x_{d1}}{C'_{OX1}} \\ &= \phi_{ms1} + 2\phi_F + \frac{qN_{CH}}{C'_{OX1}}\sqrt{\frac{2\epsilon_{si}\,(2\phi_F - V_{BS})}{qN_{CH}}}\,. \end{aligned} \tag{6.17}$$

The front gate depletion depth x_{d1} is increased by a negative body-source voltage, which results in an increased threshold voltage of partially depleted SOI-MOSFETs. The temperature dependence of the threshold voltage is then given by

$$\frac{d}{dT}V_{thPD} = \frac{d\phi_{ms1}}{dT} + \frac{d\phi_F}{dT}\left(1 + \frac{q}{C'_{OX1}}\sqrt{\frac{\epsilon_{si}N_{CH}}{kTln\left(N_{CH}/n_i\right)}}\right) . \tag{6.18}$$

In FD state, the depletion charge within the channel is constant and determined by t_{SI} and the film doping concentration N_{CH} [Col04]. The temperature dependence of the threshold voltage is then determined by the metal-semiconductor work function difference ϕ_{ms1} and the Fermi potential ϕ_F. The temperature dependence of the threshold voltage of a fully depleted SOI-MOSFET therefore results in [Col04]

$$\frac{d}{dT}V_{thFD} = \frac{d}{dT}\left(\phi_{ms1} + 2\phi_F\right) . \tag{6.19}$$

The temperature coefficient of the threshold voltage of fully depleted devices is smaller compared to partially depleted devices. This is due to the fact that in fully depleted devices, the depletion depth x_{d1} does not vary with a change in operating temperature. The threshold voltage drop of fully depleted devices with increasing temperature is therefore almost linear.

The threshold voltage was investigated experimentally for NHGATE and PHGATE devices and is shown in Figures 6.9 and 6.10, respectively. The measurements were carried out with a drain-source voltage of $|V_{DS}| = 0.1\,\mathrm{V}$, using the tangent method at the point of maximum slope in the linear I_d/V_{GS} characteristic input curve. The back gate voltage of the NHGATE and PHGATE devices is $V_{BGS} = 0\,\mathrm{V}$ and $V_{BGS} = -5\,\mathrm{V}$, respectively.

In Figure 6.9, the threshold voltage of an N-channel SOI-MOSFET is shown over temperature and body-source voltage V_{BS}. In good compliance with the results obtained priorly, there is a change in threshold voltage slope for a body-source voltage of $V_{BS} = 0\,\mathrm{V}$, located at a temperature of approximately 150 °C. There is a transition from fully depleted to partially depleted at the transition temperature T_t, from where the threshold voltage starts to decrease non-linearly. At this point, the variation of x_{d1} with temperature dominates the temperature dependency of the threshold voltage. At a temperature of 400 °C, the remaining threshold voltage is approximately 150 mV, which results in significant device channel leakage currents in analog circuits.

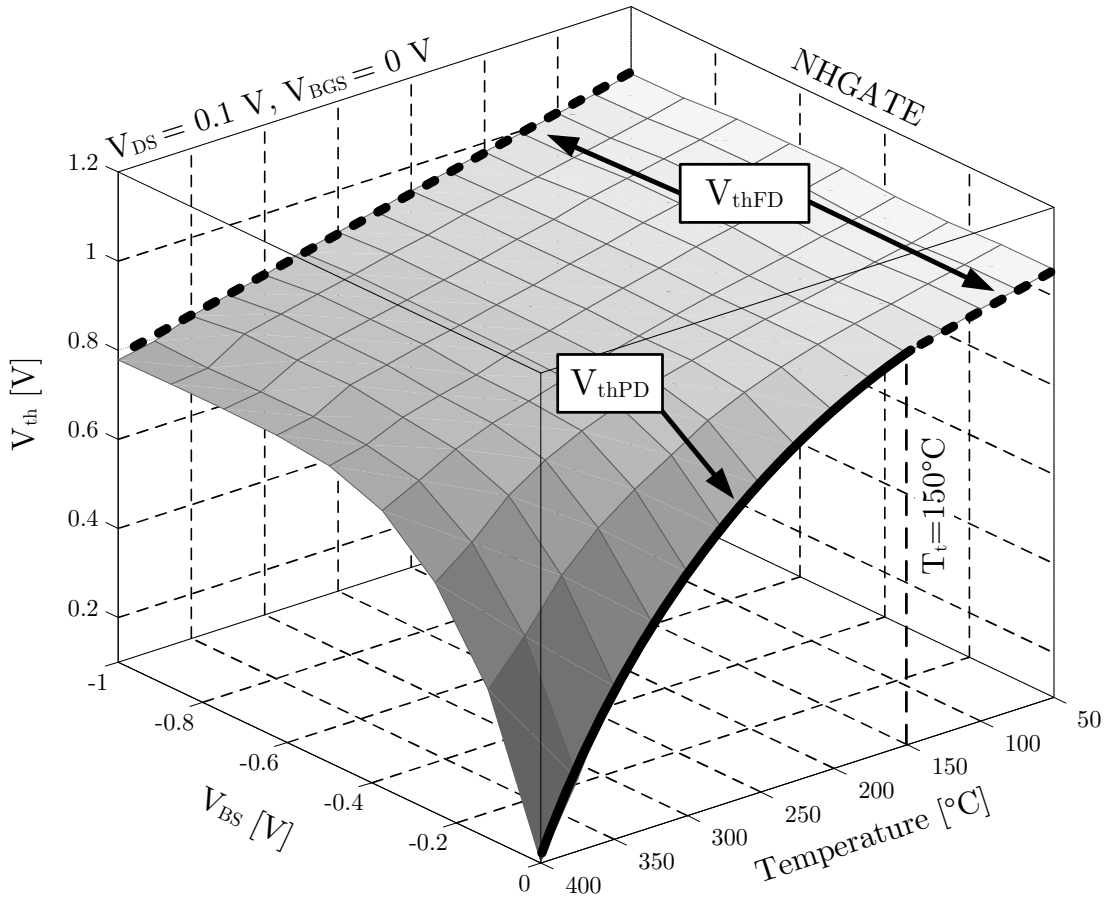

Figure 6.9: Extracted threshold voltage of an N-channel SOI-MOSFET over temperature and body-source voltage V_{BS}.

By applying a negative body-source voltage of $V_{BS} = -1\,\mathrm{V}$, the transition point is shifted to higher temperatures, whereby a lower temperature dependency in good compliance with Equation (6.19) can be recognized. The threshold voltage decreases linearly with temperature, which indicates that the device is fully depleted in the considered temperature range. With the use of RBB at 400 °C, a remaining threshold voltage of 800 mV is measured. It can also be seen here that the calculated minimum reverse bias of approximately 0.5 V seems to be sufficient to ensure full depletion of the device up to 400 °C, since the threshold voltage does not change for higher reverse bias voltages.

The threshold voltage of PHGATE devices is shown in Figure 6.10. Regular PHGATE device operation within analog circuits was considered by a back gate-source voltage of $V_{BGS} = -V_{DDA} = -5\,\mathrm{V}$, where V_{DDA} is the supply voltage. It can be seen from Figure 6.10 that in case of PHGATE devices, the transition temperature T_t for is located at approximately 300 °C. Compared to N-channel devices, the increased transition temperature is mainly related to lower channel

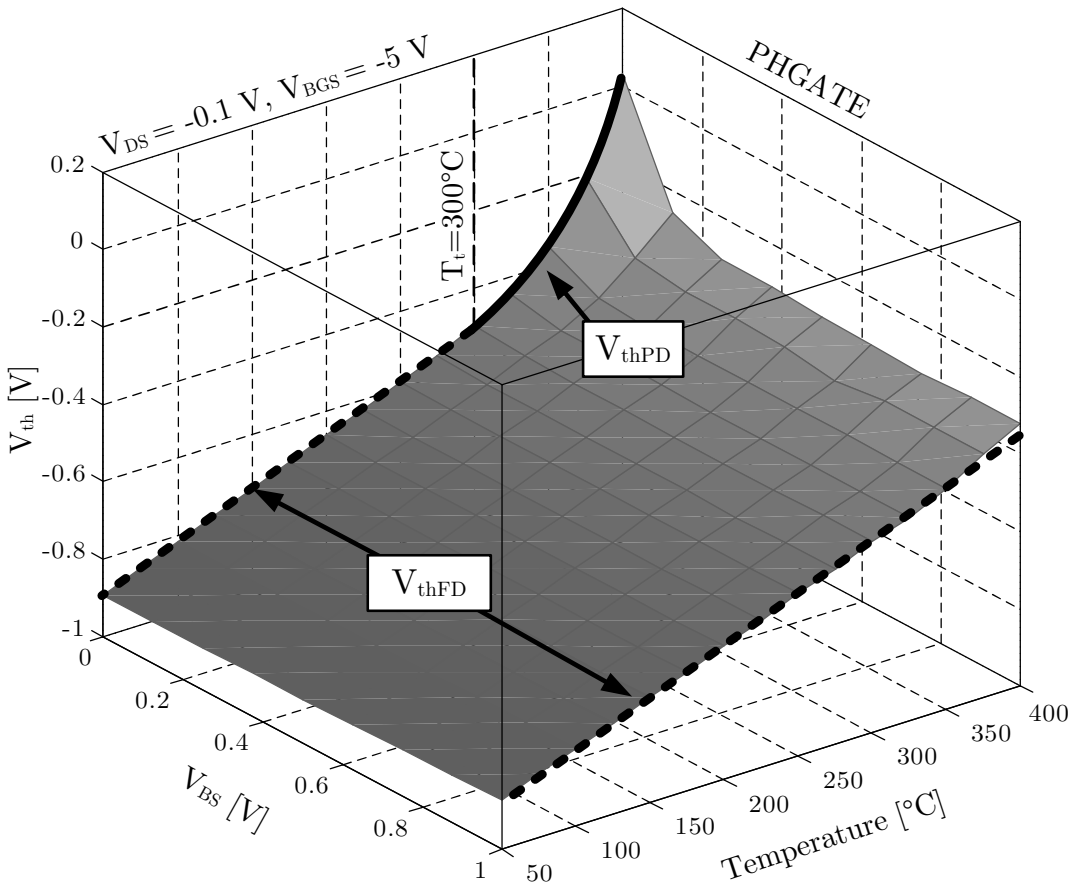

Figure 6.10: Extracted threshold voltage over temperature and body-source voltage V_{BS} of a P-channel SOI-MOSFET.

doping concentrations for P-channel devices in combination with the back gate effect. At higher temperatures, the devices also turn PD, which results in a threshold voltage of approximately 0 V at 400 °C. With applied RBB, PHGATEs remain fully depleted in the considered temperature range and a threshold voltage of −330 mV can still be achieved at 400 °C.

It was shown in this section that the use of reverse body biasing at high temperatures has a significant effect on the threshold voltage of N-channel SOI-MOSFETs and P-channel SOI-MOSFETs. Compared to threshold voltages of around 0 V without RBB, threshold voltages of 800 mV and −330 mV remain even at 400 °C for N-channel and P-channel SOI-MOSFETs, respectively.

6.7 PN-Junction Leakage Current

Three main leakage mechanisms contribute to the overall leakage current in SOI-MOSFETs, namely the PN-junction leakage current I_{PN}, the subthreshold leakage

current I_{Sub} and the sidewall leakage current, as described in Section 4.3. The sidewall leakage current of HGATE devices is effectively suppressed by the use of the H-shaped gate. For Split-Source SOI-MOSFET devices, the sidewall leakage current is suppressed by the insertion of the body contact at each side of the source region, as it was discussed in Section 3.8.3.

Short channel effects (SCE) are neglected in this work, since long channel devices with a channel length in the range of several microns are usually used for analog circuit design. The PN-junction leakage current I_{PN} is related to the reverse biasing of the drain-film PN-junction. Two components contribute to the PN-junction leakage current, i.e. the diffusion current I_{DIFF} and the generation current I_G [Col04].

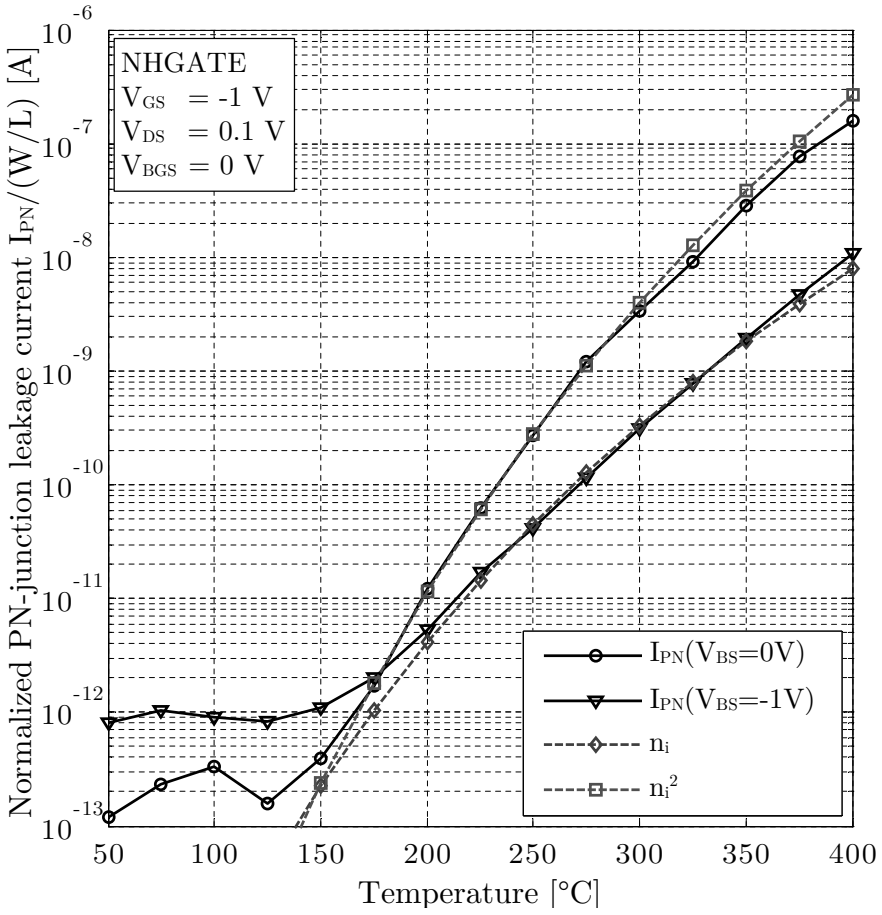

Figure 6.11: Normalized PN-junction leakage current of an NHGATE SOI-MOSFET at a gate-source voltage $V_{GS} = -1\,\mathrm{V}$ and a drain-source voltage of $V_{DS} = 0.1\,\mathrm{V}$ without RBB (circles) and with applied RBB (triangles).

The PN-junction leakage current was also investigated using RBB. It was extracted at a gate-source voltage of $V_{GS} = -1\,\mathrm{V}$ and is shown over temperature

in Figure 6.11. In case no RBB is applied, the PN-junction leakage current is proportional to n_i^2, which indicates the dominating diffusion current I_{DIFF} inside the device. With applied RBB, the leakage current reduces and is then proportional to n_i.

With applied RBB, the remaining generation current I_G is the dominating part of the PN-junction leakage current. The diffusion mechanism is prevented effectively as no proportionality to n_i^2 can be recognized in the remaining leakage current [RLK+99]. It can be concluded from these results that the device is switching from partially depleted to fully depleted when RBB is applied. With applied RBB, the generation current I_G increases to its maximum I_{Gmax} as the depletion depth inside the silicon film extends to the back interface of the device. The remaining leakage current $I_{PN}|_{FD}$ is given by Equation (6.20).

$$I_{PN}|_{FD} = I_{Gmax} = \frac{t_{SI} \cdot W \cdot L \cdot q \cdot n_i}{\tau_g} \tag{6.20}$$

Nevertheless, it can be seen from Figure 6.11 that the overall normalized PN-junction leakage current is decreased by more than one order of magnitude when RBB is applied at high temperatures.

6.8 Subthreshold Leakage Current

In comparison to the PN-junction leakage current, the subthreshold leakage current has a strong dependency on the gate-source voltage and is once again given in Equation (6.21).

$$I_{Sub} = \mu_0 C'_{OX1} \frac{W}{L} (n-1) V_t^2 exp\left(\frac{V_{GS} - V_{th}}{n \cdot V_t}\right) \left[1 - exp\left(-\frac{V_{DS}}{V_t}\right)\right] \tag{6.21}$$

Since the threshold voltage increases and the body factor n decreases, the subthreshold leakage current is expected to reduce in case RBB is applied to the SOI-MOSFET. The input characteristics of N-channel SOI-MOSFETs and P-channel SOI-MOSFETs are shown in Figures 6.12 a) and b), respectively.

For N-channel SOI-MOSFETs and P-channel SOI-MOSFETs with a back gate-source voltage of $V_{BGS} = 0\,\mathrm{V}$, the subthreshold current is negligible for a gate-source voltage of $V_{GS} = 0\,\mathrm{V}$, i.e. when the devices are turned off. For PHGATEs, an additional threshold voltage reduction has to be considered for the operation within analog circuits. With the use of RBB, the subthreshold leakage current is reduced significantly especially at high temperatures. The remaining

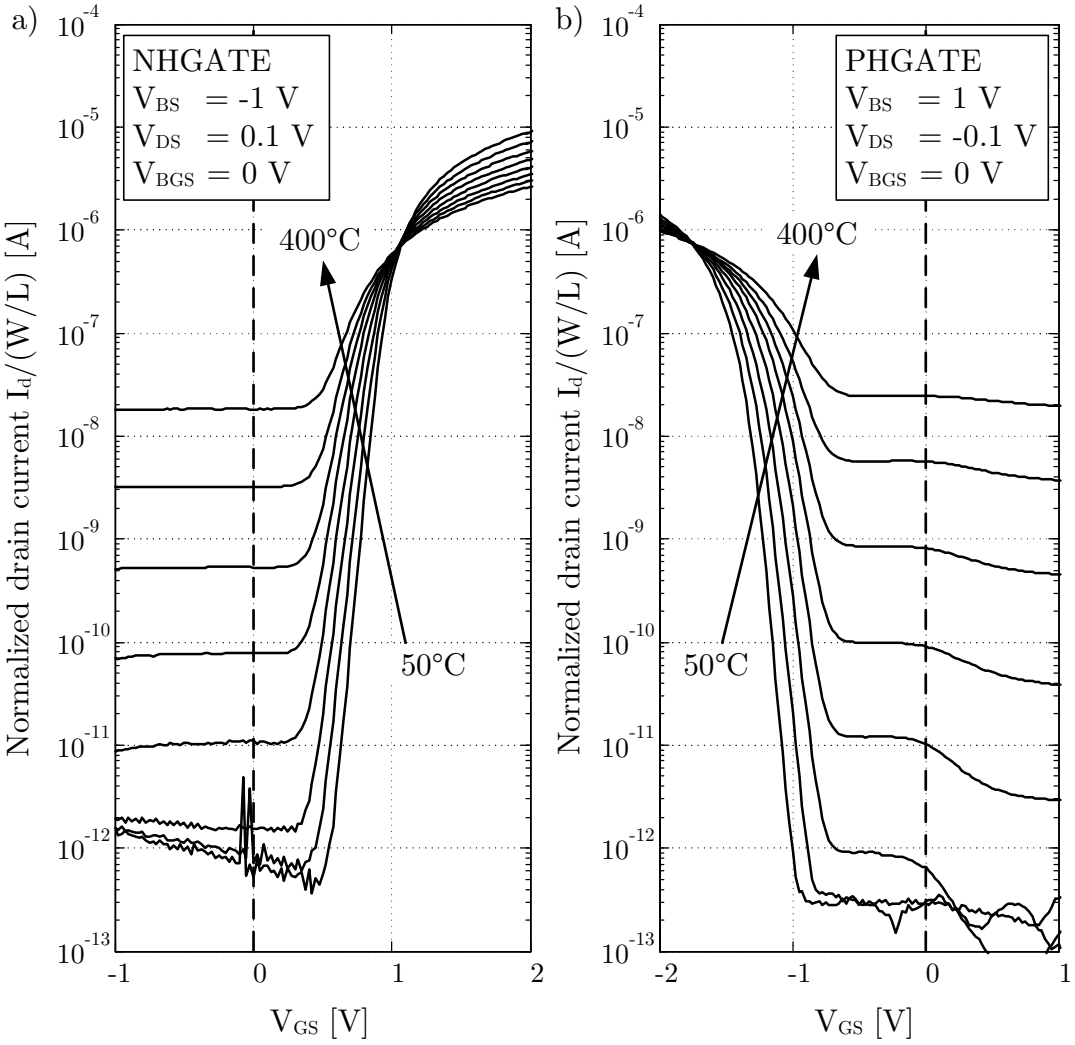

Figure 6.12: Normalized input characteristics $I_d/(W/L)$ over V_{GS} of a) N-channel SOI-MOSFET and b) P-channel SOI-MOSFET. The drain-source voltage is $|V_{DS}| = 0.1\,\mathrm{V}$, the body-source voltage is $|V_{BS}| = 1\,\mathrm{V}$ and the back gate-source voltage is $|V_{BGS}| = 0\,\mathrm{V}$.

device leakage current is the generation current portion of the PN-junction leakage current, which shows a small dependency on the applied drain-source voltage in case the device is fully depleted.

6.9 Output Conductance in Off-State

The output conductance of turned off HGATE SOI-MOSFET devices is investigated in this section. The investigation is especially interesting for analog switch applications. It was demonstrated in the last section that the remaining device

leakage current when RBB is applied is the PN-junction leakage current. This leakage current cannot be eliminated by circuit design measures. Nevertheless, it can be compensated in case the leakage current flowing onto a node is compensated by another leakage current flowing off the same node. While leakage currents flowing onto a circuit node are generated by the drain-body PN-junction of P-channel devices, leakage currents flow off a node are generated by the drain-body PN-junction of N-channel devices. Leakage current compensation can be realized when the PN-junction leakage current of both devices matches exactly. In that case, the voltage dependency of the PN-junction leakage current needs to be minimized, in order to achieve the matching of leakage current over the voltage range from ground to V_{DDA}. This can be achieved with a low output conductance.

The output conductance is given by Equation (6.22) and can be obtained experimentally from the output characteristics of N-channel SOI-MOSFETs and P-channel SOI-MOSFETs [Bin07a].

$$g_{ds}\left(V_{GS1} = 0\,\mathrm{V}\right) = \frac{\partial I_d}{\partial V_{DS}} \tag{6.22}$$

The output conductance for a gate-source voltage of $V_{GS} = 0\,\mathrm{V}$ was investigated as a function of drain-source voltage V_{DS} for a temperature of 350 °C and is shown in Figure 6.13.

If no RBB is applied, both devices show a high output conductance due to a strong voltage dependency of the subthreshold leakage current. The output conductance drops below $10\,\mathrm{nA\,V^{-1}}$, when the subthreshold leakage current is fully established ($V_{DS} \gg V_t$). If RBB is applied to both devices, the output conductance is reduced to 100 pA for the NHAGTE and to 300 pA for the PHGATE. There is no visible increase of the output conductance at low drain-source voltages in case of the reverse biased NHGATE. Due to a fully depleted film, the PN-junctions leakage current dominates the drain current of the device, which is not modulated by the drain-source voltage. In case of the PHGATE, a small increase in output conductance can be seen at low drain-source voltages. Since the measurements were taken with an effective back gate effect of $V_{BGS} = -5\,\mathrm{V}$, the threshold voltage is approximately $-300\,\mathrm{mV}$ as shown before in Figure 6.10 and the subthreshold current cannot be eliminated completely by the applied RBB voltage. As a result, an increased output conductance still exists for PHGATE devices at low drain-source voltages. Nevertheless, a significant reduction of the output conductance can be achieved when RBB is applied. The resulting leakage currents are less dependent on drain-source voltages, which benefits the compensation of leakage currents.

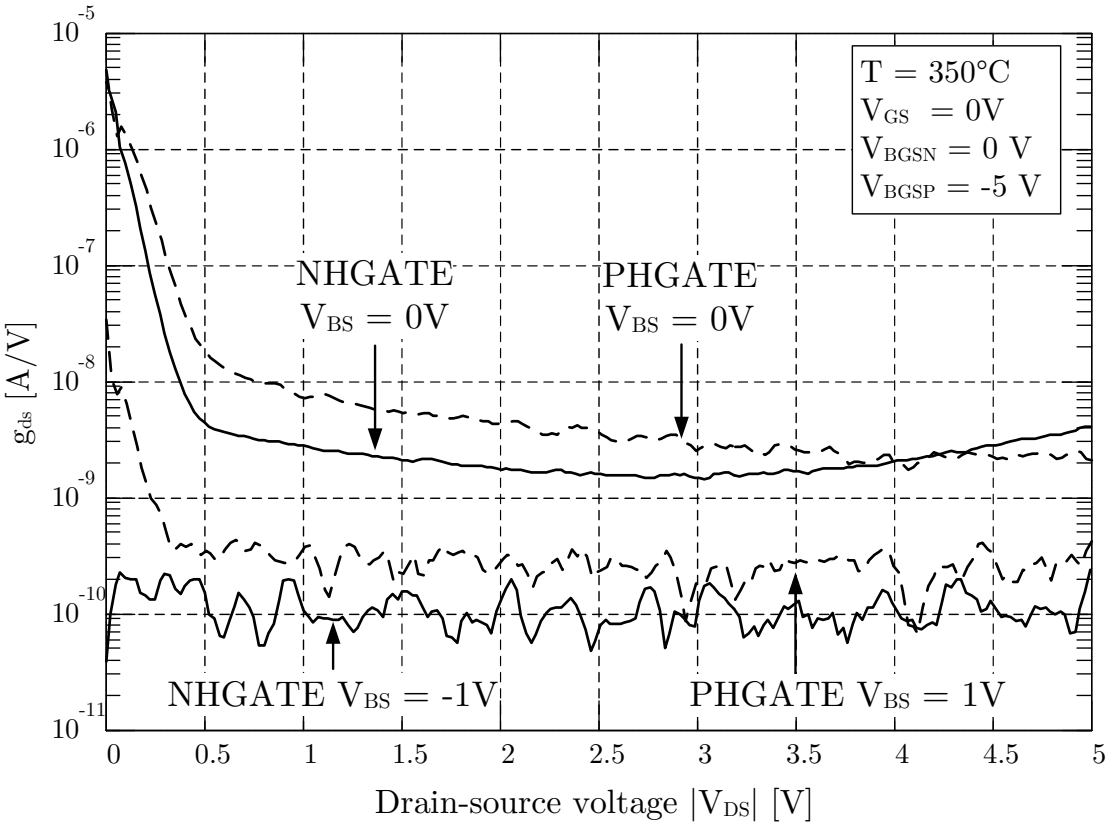

Figure 6.13: Output conductance of NHGATE and PHGATE SOI-MOSFETs with a gate-source voltage of $V_{GS} = 0\,\mathrm{V}$ at a temperature of 350 °C.

6.10 Body Current

An analysis of the body-current with and without applied RBB is presented in this section. The investigation provides measurement results of all MOSFET terminals in order to resolve the relationship between currents inside the MOSFET device. Results of the device currents as a function of V_{GS} in N-channel SOI-MOSFETs are shown in Figures 6.14 a) and 6.14 b).

The measurements were carried out on a wafer prober with a thermo chuck, which is described in more detail in appendix A.3. The maximum measurement temperature of the measurement setup is 300 °C. When the device is operated without RBB at a temperature of 300 °C, as shown in Figure 6.14 a), a high subthreshold current is active in the device channel. Thereby the major portion of the drain current is flowing in the weak inverted channel of the device. The body current below threshold is equal to the leakage current of the reverse biased drain-body PN-junction. By applying a reverse bias, generated holes are preferably transfered to the body contact. In this case two reverse biased diodes are active inside the SOI-MOSFET device, which results in a higher body current.

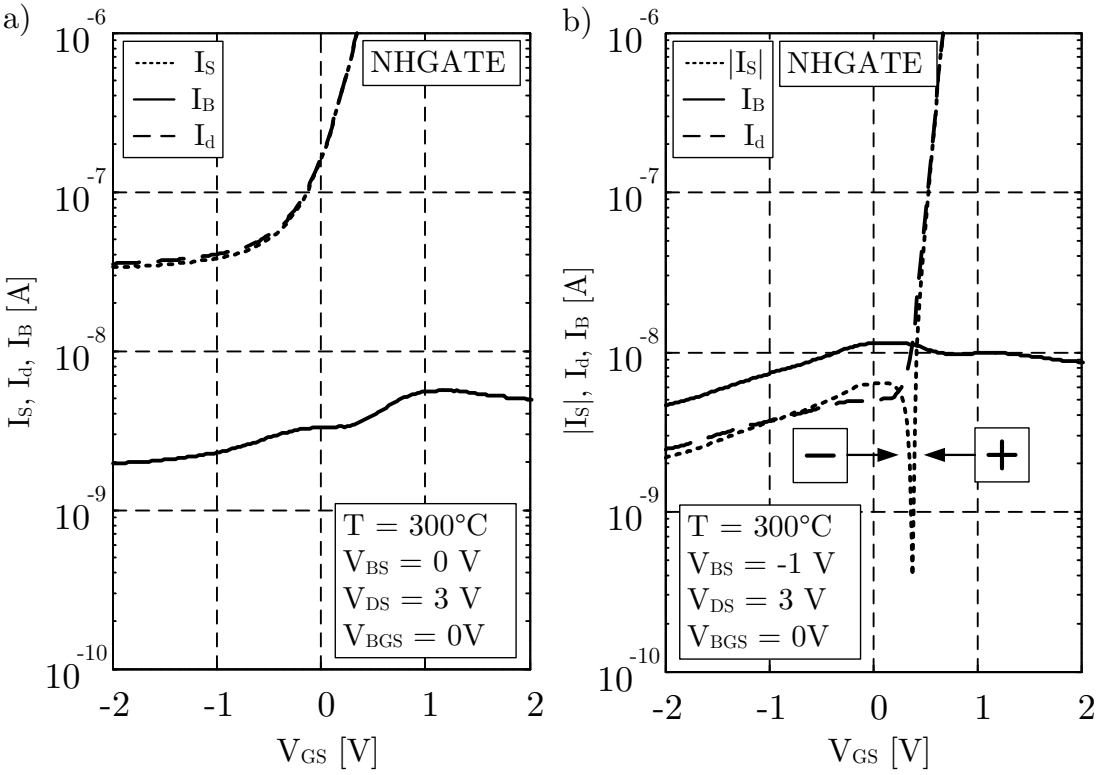

Figure 6.14: Measurement of drain current I_d, source current I_S and body current I_B over gate-source voltage V_{GS}. a) at 300 °C without RBB. b) at 300 °C with applied RBB.

If the device is reverse biased and the gate-source voltage is below threshold, as shown in Figure 6.14 b), one can see that the source current is now negative, meaning current is flowing through the reverse biased source-body diode into the source terminal. The resulting body current is then the sum of the drain current and the source current. As the device is turned on by an increase of the gate-source voltage, the source current switches it's direction due to the much higher channel current. The drain current decreases dramatically since diffusion and subthreshold leakage is reduced by the applied reverse body bias. Whether the resulting currents in reverse body biased condition are related to diffusion or generation mechanisms, can be determined by the measurements of the currents over temperature. The measured currents over temperature are shown in Figure 6.15.

In Figure 6.15, all currents were measured with a gate-source voltage of $V_{GS} = -1\,\mathrm{V}$ so that the subthreshold current is negligible in this case. The temperature slope of n_i and n_i^2 was shown in Figure 6.11 where n_i^2 has a much higher slope compared to n_i. If no RBB is applied, drain and source currents are proportional to n_i^2, whereby the diffusion mechanism is dominating. The body current on the other hand is proportional to n_i, i.e. a generation current is

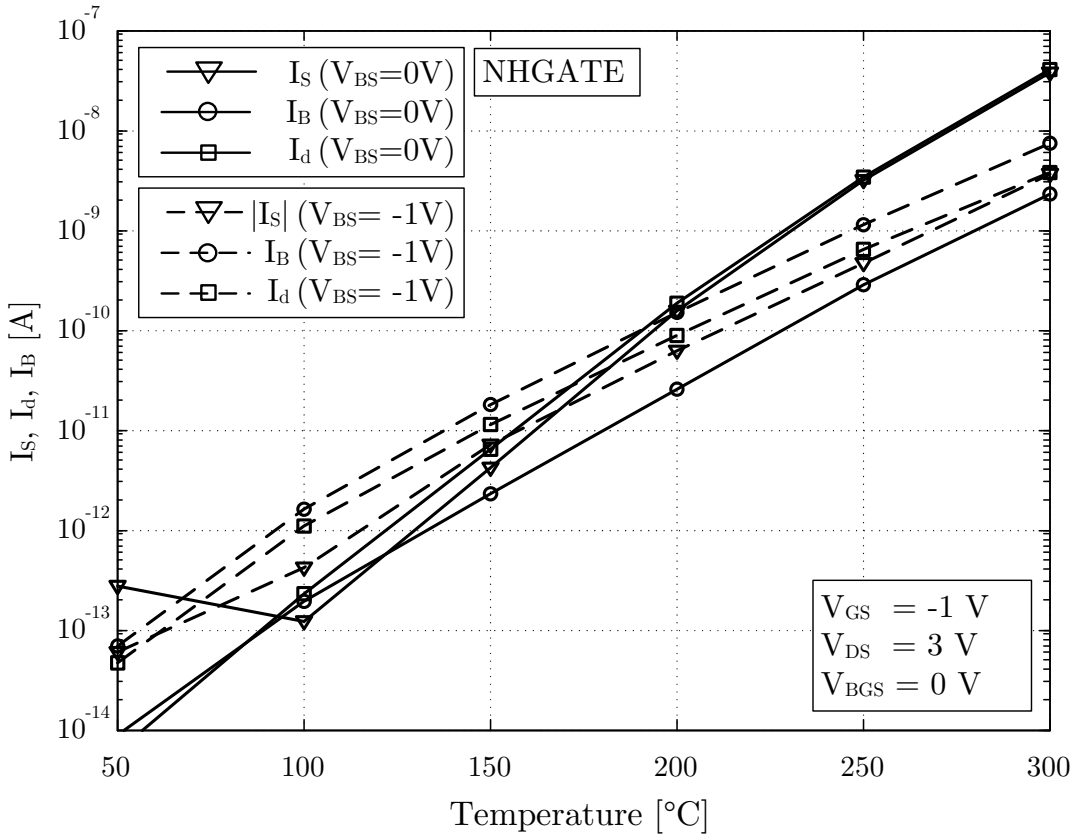

Figure 6.15: Measurement of drain current I_d, source current I_S and body current I_B over temperature with and without applied RBB.

measured at the body terminal. The body- and source currents increase if a reverse bias is applied to the device, whereby the source current is negative, as discussed before. As there is no inverted channel present in the device, the drain current is reduced significantly. The remaining effective leakage mechanism affecting the drain terminal is the generation current of the reverse biased body-drain diode. The significant reduction of device leakage currents is a big improvement of the device's I_{ON}/I_{OFF} ratio as we will see in the next section and is also a requirement for the use of the operating point in moderate inversion at high temperatures.

6.11 I_{ON}/I_{OFF} Ratio

The I_{ON}/I_{OFF} ratio of HGATE devices in the considered SOI technology was already investigated in Section 4.5. Since leakage currents are decreased significantly when RBB is applied, an increase of the I_{ON}/I_{OFF} ratio of both N-channel and P-channel SOI-MOSFETs is expected. In this section, the I_{ON}/I_{OFF}

ratio over temperature is now investigated using RBB. The saturation current of an SOI-MOSFET is once again written in Equation (6.23).

$$I_{ON} = I_{dsat} = \frac{1}{2n}\left(\frac{W}{L}\right)\mu_0 C_{OX1}\left(V_{DDA} - V_{th}\right)^2 \tag{6.23}$$

When RBB is applied to the SOI-MOSFET devices, the body factor n reduces to approximately 1.1, since the devices are fully depleted as shown in Section 6.5. This reduction leads to a small increase of saturation current, which is encountered by the increase of threshold voltage. The off-state current I_{OFF} of both devices with applied RBB is reduced to the PN-junction leakage current, as it was shown in the previous section . Since the devices remain fully depleted up to 400 °C, the off-state PN-junction leakage current is dominated by the generation current I_G.

$$I_{OFF} = I_G = \frac{t_{SI} \cdot W \cdot L \cdot q \cdot n_i}{\tau_g} \tag{6.24}$$

The measured I_{ON}/I_{OFF} ratio with and without applied RBB over temperature is shown in Figure 6.16.

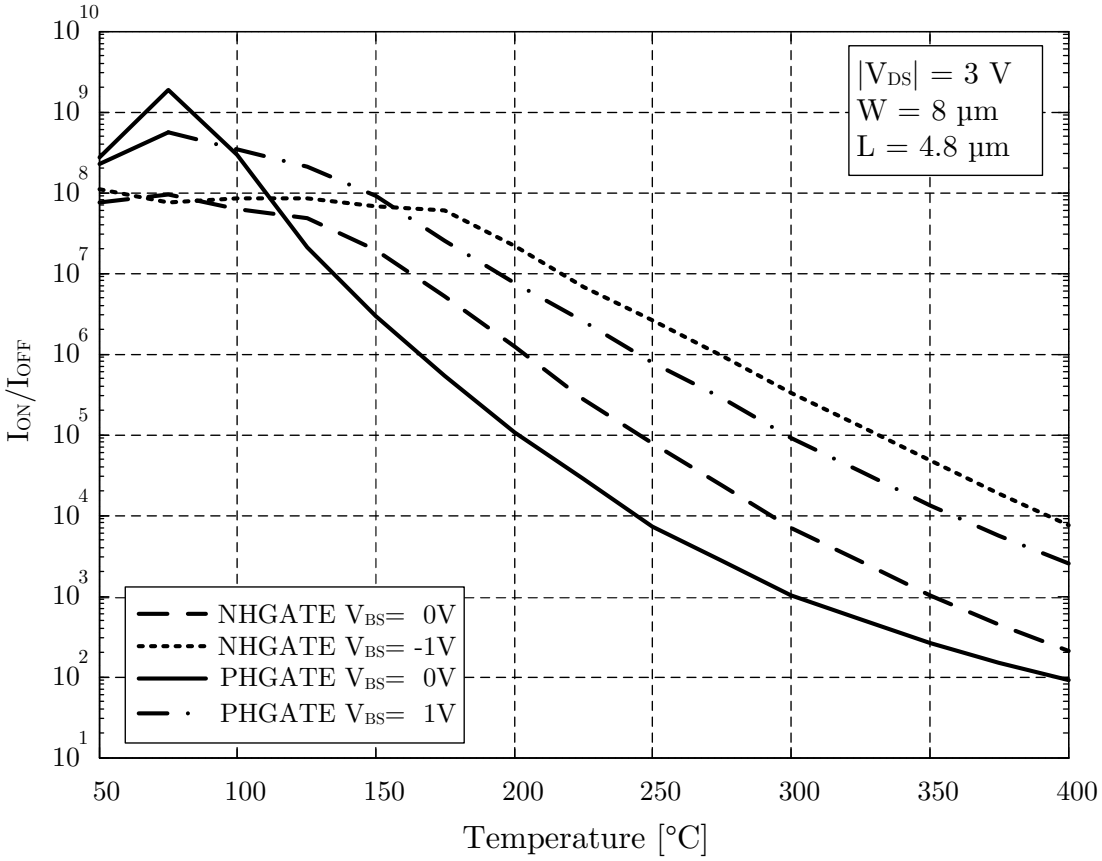

Figure 6.16: I_{ON}/I_{OFF} ratio of N-channel SOI-MOSFETs and P-channel SOI-MOSFET over temperature with and without applied RBB.

It can be seen from Figure 6.16 that the I_{ON}/I_{OFF} ratio of non-biased N-channel devices starts to decrease rapidly at temperatures above 125 °C. Above that temperature, the I_{ON}/I_{OFF} ratio is increased by approximately two decades, i.e. by a factor of approximately 100 when RBB is applied to the NHGATE SOI-MOSFET. Similar results were obtained for the P-channel SOI-MOSFET. Here, the I_{ON}/I_{OFF} ratio is increased also by a factor of approximately 100 at higher temperatures.

6.12 g_m/I_d Factor

As it was discussed in Chapter 3, the g_m/I_d factor is an important figure of merit as it determines intrinsic gain and intrinsic bandwidth of SOI-MOSFET devices. It was shown in Section 4.4.1 that the g_m/I_d factor is strongly dependent on the operating temperature and decreases significantly as leakage current inside the SOI-MOSFET increase. Due to the influence of leakage currents at high temperatures, the g_m/I_d factor is very low, especially in the weak inversion range and the moderate inversion range.

In this section, the g_m/I_d factor is investigated with the use of RBB. As RBB reduces device leakage currents, an influence on the g_m/I_d factor is also expected. The g_m/I_d factor with and without RBB was extracted experimentally using the extraction method already described in Section 4.4.1. The results are shown in Figures 6.17 a) and 6.17 b) for the NHGATE SOI-MOSFET without and with applied RBB, respectively.

In Figure 6.17 a), the priorly extracted g_m/I_d factor without RBB is shown again for better comparison. To provide sufficient safety margin to the leakage current level, normalized operating currents of ten times the leakage current level are chosen. The lowest feasible operating current is the desired point of operation for high gain applications. Without RBB, the lowest feasible operating point up to 350 °C is at a normalized drain current of $I_d/(W/L) = 300\,\text{nA}$. At this operating current, the g_m/I_d factor reaches $12\,\text{V}^{-1}$ at 50 °C and $2.9\,\text{V}^{-1}$ at 350 °C. In case a maximum operating temperature of 400 °C is required, the minimum normalized operating current is $I_d/(W/L) = 1.5\,\mu\text{A}$. At this point, g_m/I_d factors of $3.3\,\text{V}^{-1}$ and $0.8\,\text{V}^{-1}$ are reached at 50 °C and 400 °C, respectively.

The g_m/I_d factor of the NHAGTE SOI-MOSFET with applied RBB is shown in Figure 6.17 b). First of all, at low temperatures it can be recognized that the g_m/I_d factor in the weak inversion region does not vary with drain current as much as in the non-biased condition. This is related to the fact that the body factor n does

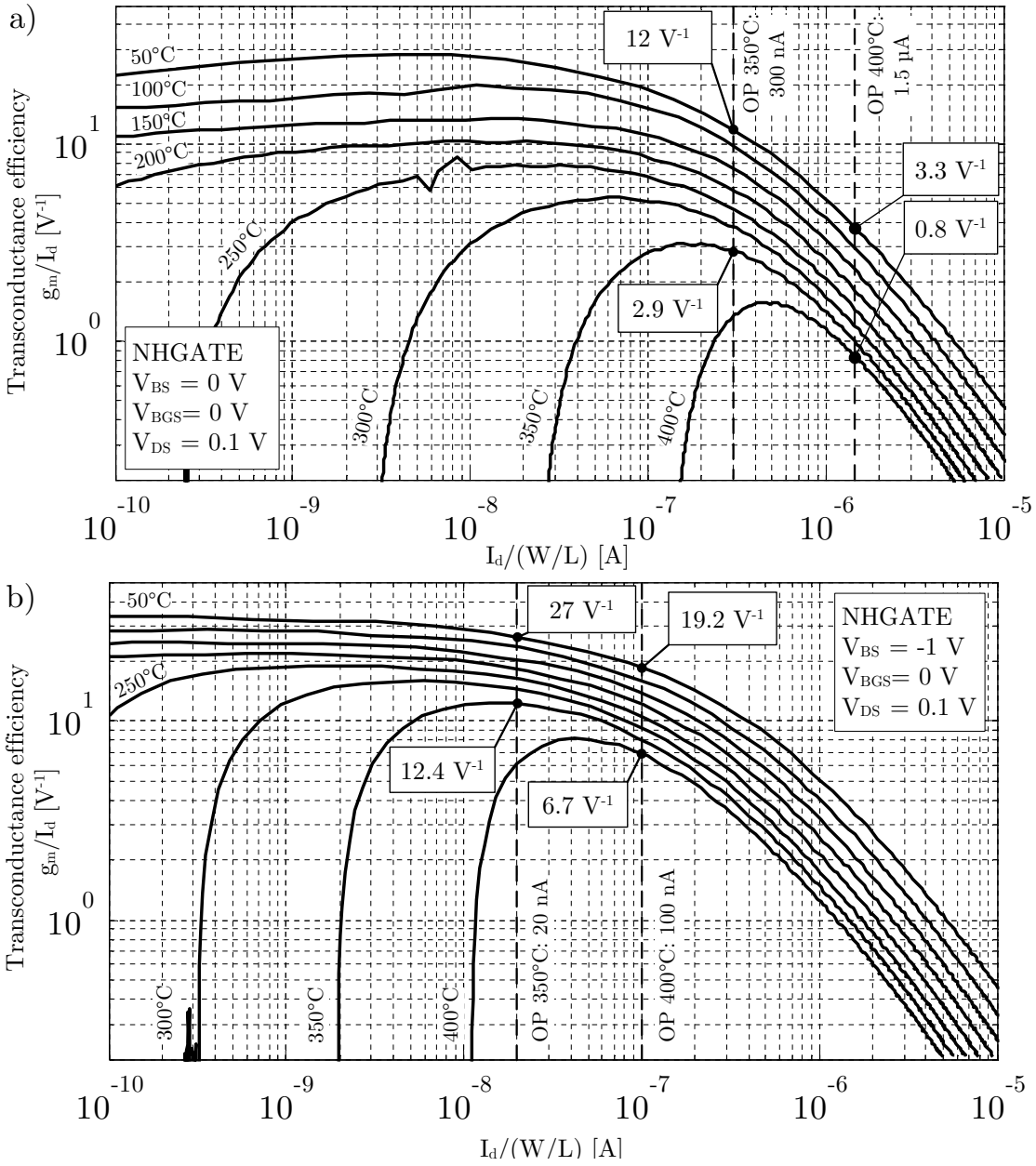

Figure 6.17: Measured g_m/I_d over normalized drain current $I_d/(\mathrm{W/L})$ of an NHGATE SOI-MOSFET for different temperature up to 400 °C with a drain-source voltage of $V_{DS} = 0.1\,\mathrm{V}$ and a back gate-source voltage of $V_{BGS} = 0\,\mathrm{V}$. a) without RBB b) with applied RBB.

not change with increased gate-source voltage in fully depleted SOI-MOSFETs since the film of the SOI-MOSFET device is already depleted completely. The g_m/I_d value in weak inversion is given by Equation (6.25) [Bin07b].

$$\left.\frac{g_m}{I_d}\right|_{WI} = \frac{1}{nV_t} \tag{6.25}$$

It decreases only by the influence of the thermal voltage V_t. The value of the body factor n can be extracted using Equation (6.25). Solving Equation (6.25) for n yields

$$n\,(50\,^{\circ}\mathrm{C}) = \left(\left.\frac{g_m}{I_d}\right|_{WI} \cdot V_t \right)^{-1} = \left(33.64\,\mathrm{V}^{-1} \cdot 27.84\,\mathrm{mV}\right)^{-1} = 1.08\,. \tag{6.26}$$

The extracted value of the body factor is in good agreement with the prior results and indicates that the device is fully depleted. With increasing temperature, the g_m/I_d factor decreases linearly due to the linear increase in thermal voltage. At a temperature of 250 °C, leakage currents start to influence the operation of the device in the weak inversion region. Nevertheless, it can be concluded from these measurements that the device can be safely operated up to 250 °C with a normalized operating drain current of 1 nA, i.e. in the weak inversion region. For an operating temperature of 350 °C, a minimum normalized drain current of 20 nA is specified to operate the device. At this point, a g_m/I_d factor of 27 V^{-1} and 12.4 V^{-1} is reached at 50 °C and 350 °C, respectively. In case an operating temperature of 400 °C is required for the application, the minimum normalized drain current is 100 nA, resulting in a g_m/I_d factor of 19.2 V^{-1} and 6.7 V^{-1} at 50 °C and 400 °C, respectively.

The g_m/I_d factor over normalized drain current $I_d/(W/L)$ of PHAGTE SOI-MOSFETs is shown in Figures 6.18 a) and 6.18 b) without and with applied RBB, respectively. The drain-source voltage is $V_{DS} = -0.1\,\mathrm{V}$ and the back gate-source voltage is $V_{BGS} = -5\,\mathrm{V}$. In case no RBB is applied, as shown in Figure 6.18 a), a minimum normalized operating current of 1.2 µA is feasible at a temperature of 350 °C. At this operating point, the g_m/I_d factor reaches 1.5 V^{-1} and 0.45 V^{-1} at 50 °C and 350 °C, respectively. In case a maximum operating temperature of 400 °C is required, the minimum normalized operating current is $I_d = 3\,\mu\mathrm{A}$. At this point a g_m/I_d factor of 0.49 V^{-1} and 0.15 V^{-1} can be reached at 50 °C and 400 °C, respectively.

By applying RBB to the PHGATE SOI-MOSFET, the leakage current level decreased significantly. The lowest feasible normalized operating current for a temperature of 350 °C is 30 nA. At this operating current, the g_m/I_d factor reaches 15.5 V^{-1} and 7.4 V^{-1} at 50 °C and 350 °C, respectively. For a maximum operating temperature of 400 °C, a normalized operating current of 100 nA is feasible and g_m/I_d reaches values of 9 V^{-1} and 3.5 V^{-1} at 50 °C and 400 °C, respectively.

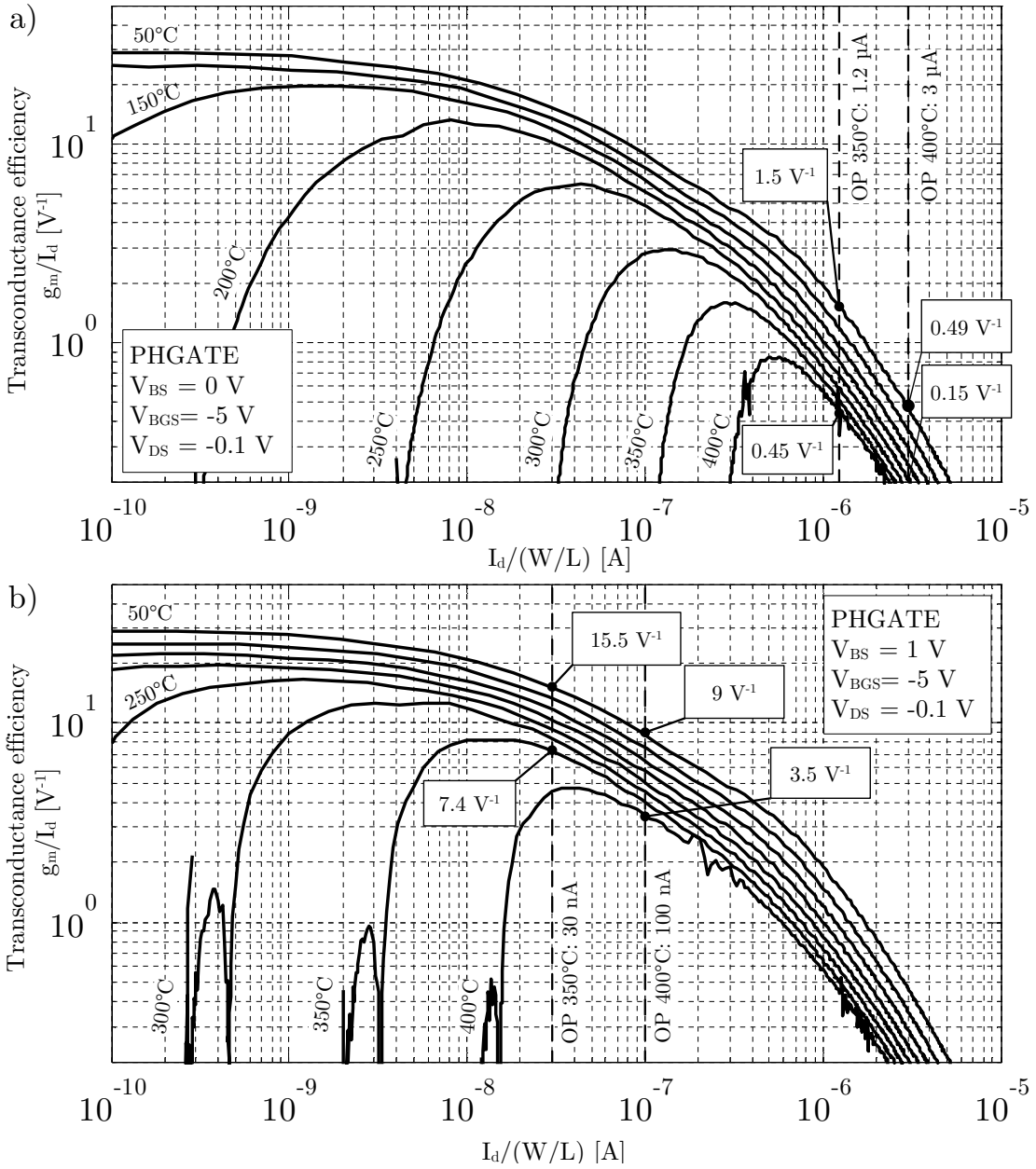

Figure 6.18: Measured g_m/I_d over normalized drain current $I_d/(\mathrm{W/L})$ of an PHGATE SOI-MOSFET for different temperature up to 400 °C with a drain-source voltage of $V_{DS} = -0.1\,\mathrm{V}$ and a back gate-source voltage of $V_{BGS} = -5\,\mathrm{V}$. a) without RBB b) with applied RBB.

The previous measurements were taken with a drain-source voltage of $|V_{DS}| = 0.1\,\mathrm{V}$. For application within analog circuits, the device has to operate at different drain-source voltages, depending on the DC operating point within the circuit. Therefore, the dependencies of the leakage current and the g_m/I_d factor on drain-source voltage is discussed below. It was shown in Section 3.8.2 that the

subthreshold leakage current is independent from the drain-source voltage in case the drain-source voltage is significantly smaller than the thermal voltage V_t. At 400 °C, the thermal voltage is $V_t = 58\,\text{mV}$ and thereby close to V_{DS}. Due to an increased subthreshold current, a small increase in leakage current is thereby expected at high drain-source voltages. This can be seen in Figure 6.19 a) for an NHGATE device without RBB.

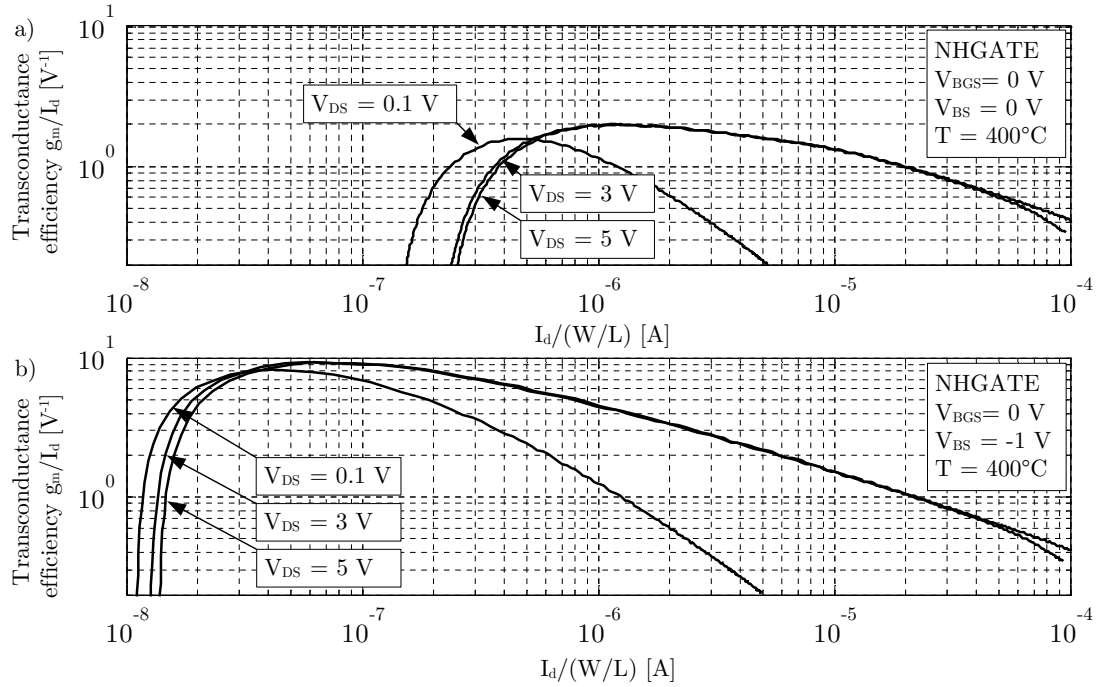

Figure 6.19: Measured g_m/I_d factor over normalized drain current $I_d/(\text{W/L})$ of an NHGATE SOI-MOSFET at 400 °C for different drain-source voltages. a) without RBB. b) with applied RBB.

A rather large increase of the leakage current due to the step from $V_{DS} = 0.1\,\text{V}$ to $V_{DS} = 3\,\text{V}$ can be seen here, whereby only a small increase can be recognized due to the step from $V_{DS} = 3\,\text{V}$ to $V_{DS} = 5\,\text{V}$. It can also be noticed from this plot that the g_m/I_d factor in strong inversion increases with increasing V_{DS}. This is related to a higher transconductance g_m for the same drain current in saturation. The reverse biased case is shown in Figure 6.19 b). There is no significant difference in the leakage current level between $V_{DS} = 0.1\,\text{V}$ and $V_{DS} = 3\,\text{V}$, which supports the assumption that there is no subthreshold leakage current present when RBB is applied.

The presented results demonstrate the relevance of the proposed method for the improvement of the analog performance of SOI-MOSFETs at high temperatures. Due to a much lower operating current and operation in the moderate inversion

region, significantly higher g_m/I_d values can be achieved also at low temperatures. For circuit operation up to 350 °C, the g_m/I_d factor of the NHGATE is improved by a factor of approximately 4.2. The operating current is still ten times larger than the leakage current level in order to provide a safety margin. At 400 °C, the g_m/I_d factor of the NHGATE can be improved by a factor of approximately 8.3. Even better results were achieved for PHGATE SOI-MOSFETs. The g_m/I_d factor of these devices is improved by factors of approximately 16.4 and 23.3 at 350 °C and 400 °C, respectively.

6.13 Technology Current

The technology current refers to the center of the moderate inversion region [Bin07a]. Thereby, knowing the exact technology current over temperature helps to understand, whether the location of the moderate inversion region is strongly dependent on temperature or not. In Section 4.4.2, an extraction method to obtain the technology current I_0, as proposed by [EHT+05], was described. It was also shown that the extraction method cannot be applied to partially depleted SOI-MOSFETs with sufficient accuracy at elevated temperatures. The reason is that both, the technology current I_0 and the body factor n change with temperature. It this case, the technology current cannot be fitted using the measured g_m/I_d curves.

In Section 6.5, measurement results for the body factor n were presented. The results represent the body factor as a function of temperature for a constant gate-source voltage. Since the channel current increases with temperature, a constant gate-source bias results in a change of the inversion state of the device. Thereby, the measured body factor does not represent the body factor in one single operating region, e.g. in weak inversion. The required weak inversion value of the g_m/I_d factor, which is necessary to extract the technology current can not be obtained from this measurement.

It was shown in the previous section that the g_m/I_d curves over normalized drain current $I_d/(W/L)$ show a much better linearity in the weak inversion region, in case RBB is applied to the device. As a result, the technology current for the reverse biased fully depleted SOI-MOSFET device can be extracted up to a temperature of 300 °C. The technology current of an NHGATE SOI-MOSFET has been extracted graphically from Figure 6.20 using the tangent method in weak inversion and strong inversion. The dots shown in this figure represent the

technology current for a specific temperature. It can be seen from this figure that the technology current decreases with increasing temperature.

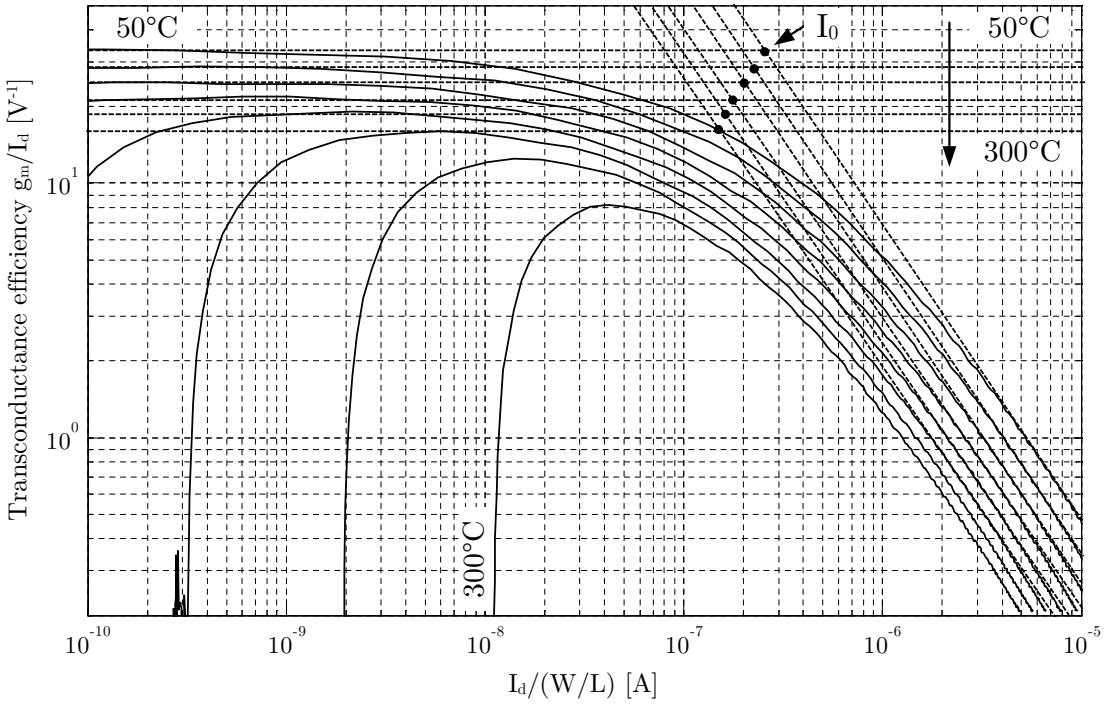

Figure 6.20: Graphical extraction method of the technology current from the g_m/I_d curves of NHGATE SOI-MOSFETs. The drain-source voltage is $V_{DS} = 0.1\,\mathrm{V}$, the back gate-source voltage is $V_{BGS} = 0\,\mathrm{V}$ and the body-source voltage is $V_{BS} = -1\,\mathrm{V}$.

The same extraction technique was used to extract the technology current of PHGATE SOI-MOSFETs. The results of both measurements are shown in Figure 6.21. The drain-source voltage of both devices is $|V_{DS}| = 0.1\,\mathrm{V}$ and the back gate-source voltages are $V_{BGS} = 0\,\mathrm{V}$ and $V_{BGS} = -5\,\mathrm{V}$ for NHGATEs and PHGATEs, respectively.

The technology current was extracted up to 300 °C and extrapolated up to 400 °C. In case of NHAGTE and PHGATE devices, it can be recognized that the technology current decreases with increasing temperature. For convenience, the expression of the technology current is written again in Equation (6.27).

$$\begin{aligned} I_0(T) &= 2\mu_0(T)\, C'_{ox1} n(T)\, V_t^2(T) \\ &= 2\mu_{T0} \left(\frac{T}{T_0}\right)^{\mathrm{BEX}} C'_{OX1} n \left(\frac{kT}{q}\right)^2 \end{aligned} \tag{6.27}$$

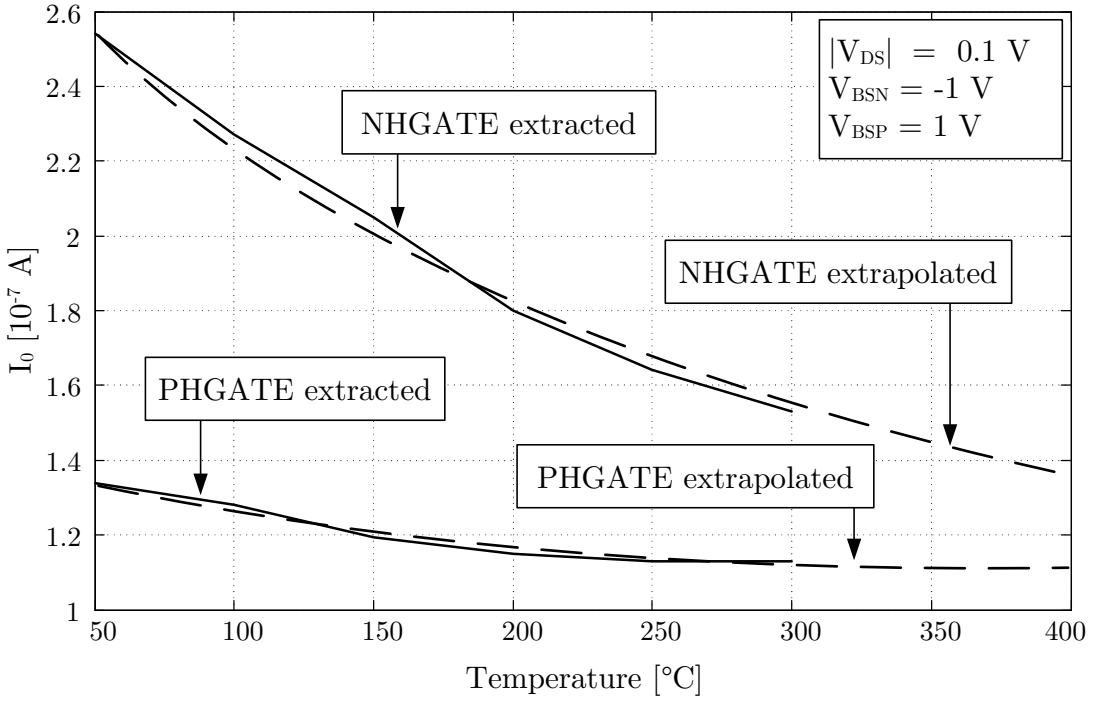

Figure 6.21: Experimentally extracted technology current I_0 of NHAGTE and PHAGTE SOI-MOSFET over temperature. The technology current was extracted up to 300 °C and extrapolated up to 400 °C.

Since n is almost constant in a fully depleted device, the thermal voltage V_t and the zero-field charge carrier mobility dominate the temperature dependency of the technology current. From the measurement results, it can be concluded that the exponent BEX is lower than -2 for both devices. Otherwise the overall temperature dependency of the technology current would be positive. Thus, in the considered technology, the zero-field charge carrier mobility μ_0 is the dominating factor in the technology current of reverse biased SOI-MOSFET devices. This result is also intuitive as both, the technology current and the zero-field charge charge carrier mobility are higher for NHAGTE devices, compared to PHGATE devices. In addition, the temperature exponent of the technology current of N-channel devices is lower than that of P-channel devices, which can be related to a lower temperature exponent of the zero-field charge carrier mobility for N-channel devices.

With the use of reverse body biasing, the technology current can be experimentally extracted from the g_m/I_d over $I_d/(W/L)$ measurements up to 300 °C. The technology current of both devices decreases with increasing temperature but does not show a variation higher than one order of magnitude in the considered temperature range. In case of NHAGTE devices, the technology current drops

from 250 nA at 50 °C to approximately 139 nA at 400 °C. When the device is biased in the mid moderate inversion region with a constant drain current, the inversion state of the transistor would shift slightly towards strong inversion with increasing temperature. Nevertheless, the shift with increasing temperature is so small that the device remains in moderate inversion. From a circuit designers perspective, one can neglect the temperature variation of the technology current for fully depleted reverse biased devices in the considered technology.

6.14 Early Voltage

The Early voltage V_A can be experimentally obtained from the output characteristics of the transistor and is given by Equation (6.28).

$$V_A = \left(\frac{\partial I_d}{\partial V_{DS} \cdot I_d} \right)^{-1} = \left(\frac{\partial ln(I_d)}{\partial V_{DS}} \right)^{-1} \tag{6.28}$$

The Early voltage was measured as a function of normalized drain current $I_d/(W/L)$ for NHGATE devices with a drain-source voltage of $V_{DS} = 4\,\mathrm{V}$. The results are shown in Figures 6.22 a) and 6.22 b) for temperatures of 350 °C and 400 °C, respectively.

Without RBB, the Early voltage of the device at 350 °C is approximately 59 V in moderate inversion and increases in the higher strong inversion region. It should be noticed from this figure that due to leakage currents, a normalized drain current of approximately 100 nA is the lowest possible drain current. Leakage currents dominate the overall channel current below that operating current.

The Early voltage is slightly decreased compared to the non-biased device when RBB is applied with $V_{BS} = -1\,\mathrm{V}$ in the moderate inversion region. The decrease is caused by a lower saturation current for reverse biased devices in the saturation region. This represents a drawback of reverse body biasing with respect to device performance optimization. Nevertheless, a benefit of the RBB technique can be recognized from Figure 6.22 b) at a temperature of 400 °C. It can be seen that the Early voltage cannot be extracted at 400 °C from devices without RBB and drain currents in the moderate inversion range. The reason is that channel leakage currents at 400 °C limit the minimum drain current to approximately 500 nA. With applied RBB, the Early voltage is 50 V at a drain current of 100 nA and a source-drain voltage of 4 V. Considering these results, it was found that RBB is a suitable solution to achieve adequate Early voltages in the lower moderate inversion region at very high temperatures.

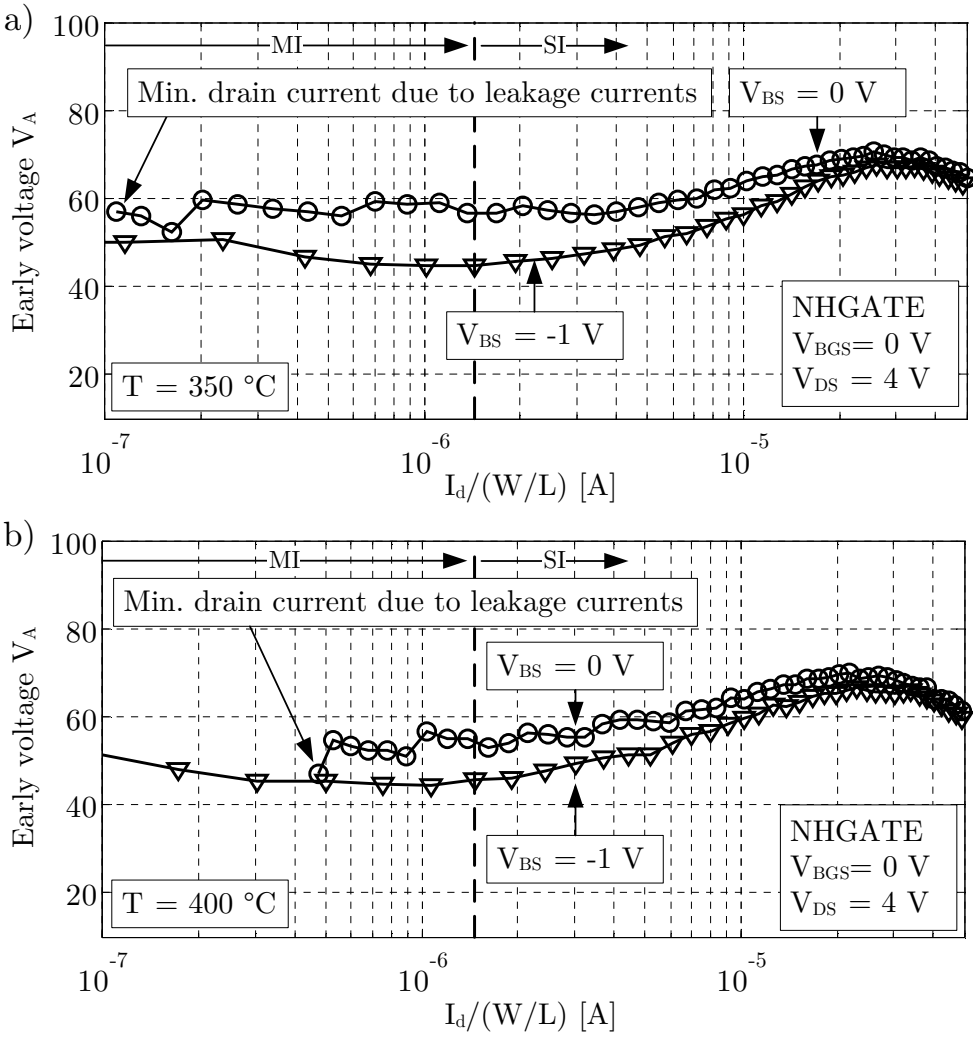

Figure 6.22: Measured Early voltage of an NHGATE device with a drain-source voltage of $V_{DS} = 4\,\mathrm{V}$ and a back gate-source voltage of $V_{BGS} = 0\,\mathrm{V}$ a) at an operating temperature of 350 °C b) at an operating temperature of 400 °C.

6.15 Intrinsic Gain and Intrinsic Bandwidth

The intrinsic gain of NHGATE and PHGATE SOI-MOSFET devices using RBB was investigated and experimental results are presented in this section. Measurements were taken with a drain-source voltage of $|V_{DS}| = 3\,\mathrm{V}$ at different temperatures up to 400 °C and are shown in Figures 6.23 a) and b) for the NHGATE without RBB and with RBB, respectively. In Figure 6.23 a), the intrinsic gain of an NHGATE without RBB is plotted against the drain current I_d for different temperatures up to 400 °C.

Considering a sufficient safety margin of approximately one decade, an operating drain current of 1 µA is chosen as the lowest possible operating current

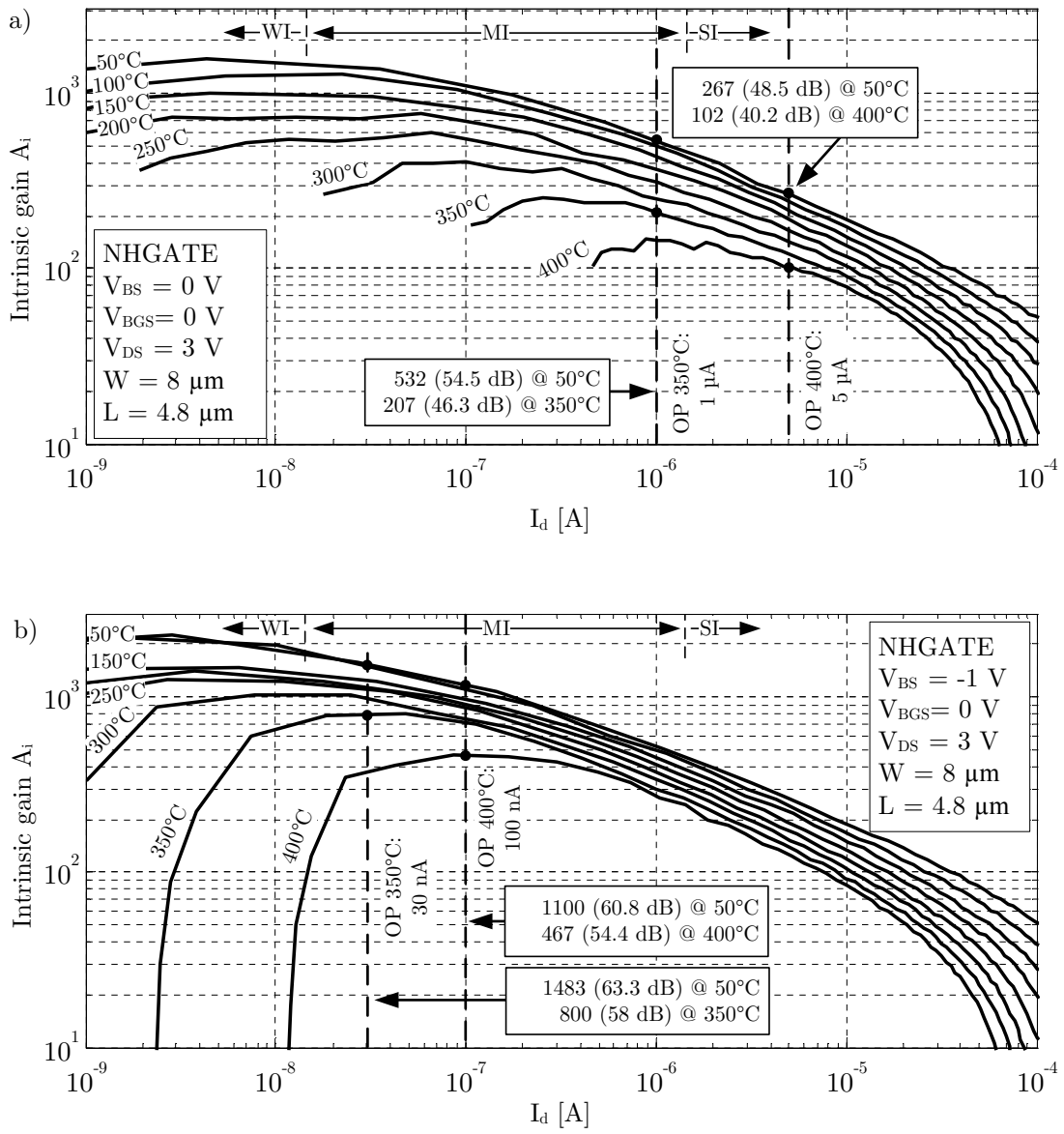

Figure 6.23: Intrinsic gain of an NHGATE SOI-MOSFET over drain current I_d at a drain-source voltage of $V_{DS} = 3\,\mathrm{V}$ at temperatures from 50 °C to 400 °C a) without RBB. b) with applied RBB.

up to 350 °C. At this operating point, which is placed at the transition from moderate inversion to strong inversion, an intrinsic gain of 46.3 dB can be reached at 350 °C. In case operating temperatures up to 400 °C are required, the operating current has to be increased up to 5 µA. An intrinsic gain value of 40.2 dB was measured at 400 °C with an operating current of 5 µA in the strong inversion region. Figure 6.23 b) shows the measured intrinsic gain with applied RBB. It can be recognized from Figure 6.23 b) that a much lower operating point can be chosen as device leakage currents are significantly smaller. In addition, a small increase of

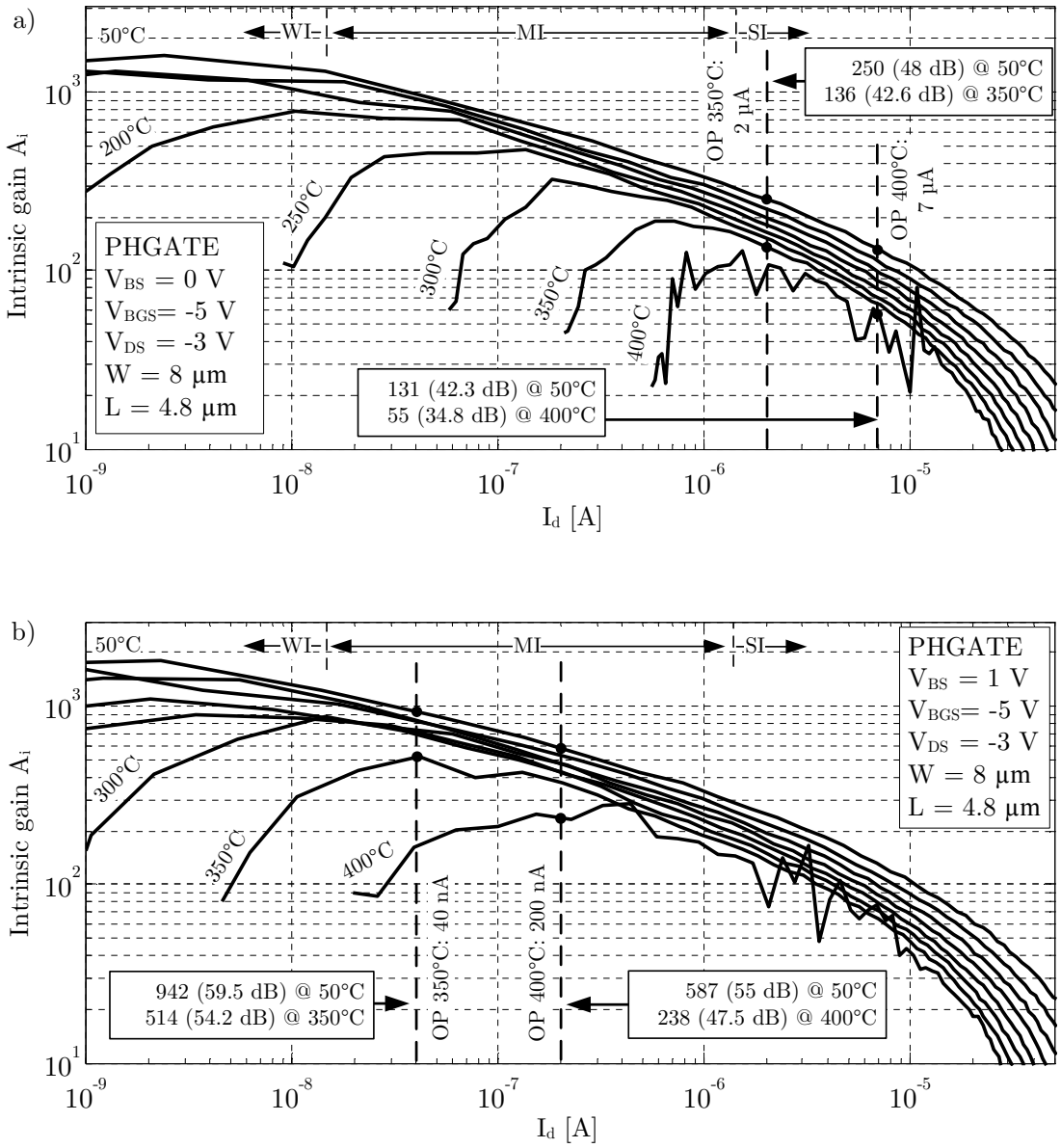

Figure 6.24: Intrinsic gain of a PHGATE SOI-MOSFET over drain current I_d at a drain-source voltage of $V_{DS} = -3\,\mathrm{V}$ at temperatures from 50 °C to 400 °C a) without RBB. b) with applied RBB.

the intrinsic gain in the weak inversion region can be seen, which results from the decreased body factor n for fully depleted SOI-MOSFETs. With the use of RBB, a drain current of 30 nA can be determined as operating point at an operating temperature of 350 °C. Compared to the non-biased device, the resulting intrinsic gain is 58 dB, with an increase of 17.8 dB. For a maximum operating temperature of 400 °C, the drain current can be reduced down to 100 nA. With the reduction of the operating current, the intrinsic gain is increased by 14.2 dB at this temperature in comparison to the con-biased case. Due to the use of RBB applied to the

NHGATE SOI-MOSFET device, the moderate inversion region can be used as operating point up to a temperature of 400 °C. In comparison, the lowest possible operating point without RBB lies in the strong inversion region, were the intrinsic gain of the SOI-MOSFET device is significantly smaller.

Figure 6.24 a) shows experimental results obtained for PHGATE SOI-MOSFETs without reverse body biasing. The back gate-source voltage V_{BGS} is −5 V. Without RBB, the lowest feasible operating point at an operating temperature of 350 °C is 2 µA, with an intrinsic gain of 42.6 dB. In case an operating temperature of 400 °C is required, the operating current has to be increased up to 7 µA, whereby an intrinsic gain of 34.8 dB is achieved.

When reverse body biasing is applied to the PHAGTE SOI-MOSFET device, the operating current at a temperature of 350 °C can be reduced down to 40 nA. At this point, an intrinsic gain of 54.2 dB is achieved using reverse body biasing, which represents an increase of 11.6 dB. Up to 400 °C, the operating current should not be chosen below 200 nA in order to remain a safety margin to the leakage current level. At this operating point, an intrinsic gain of 47.5 dB was measured. With the use of RBB, the achievable intrinsic gain at 400 °C is increased by 12.7 dB. The overall results demonstrate that the intrinsic gain of SOI-MOSFET devices is improved significantly when RBB is applied to the devices, especially in the moderate inversion region.

6.16 Body-Effect Transconductance

The body-effect transconductance g_{mb} describes the change in drain current, which results from a change in body-source voltage V_{BS} and is given in Equation (6.29) [Bin07b].

$$g_{mb} = \frac{\partial I_d}{\partial V_{BS}} \tag{6.29}$$

The drain current of the partially depleted SOI-MOSFET devices can be controlled by changing the body-source voltage. Measurement of the body-effect transconductance is only relevant for HGATE devices, since in the considered SOI technology, body and source terminal of Split-Source devices are short-circuited. For the calculation of the body-effect transconductance, the gate-source voltage as well as the drain-source voltage are held constant in the considered operating point of the device. Body-source reverse bias voltages of $V_{BSN} = -1\,\text{V}$ and $V_{BSP} = 1\,\text{V}$ were applied for N-channel HGATE devices and P-channel HGATE devices, respectively. Due to the reverse bias voltage, both devices remain fully depleted up

to 400 °C. The resulting body-effect transconductance for fully depleted devices is investigated in this section. The results are especially important for analog gain stages, e.g. common drain stages or common source stages with degenerated source effect, where intrinsic gain can be decreased due to body-effect transconductance [Bin07b]. Another important question for the investigation of the body-effect transconductance is how the drain current of the device is affected by noise on the body-contact in case the RBB voltage is generated on chip.

For the following investigation, the body-effect transconductances for NHGATE and PHGATE devices were measured with a gate-source voltage of $V_{GS1} = 0\,\mathrm{V}$. Results are shown in Figure 6.25 a). The transition from partially depleted to fully depleted can be clearly seen in Figure 6.25 a). As expected, the influence of body-source voltage on the drain current is much lower when the device is fully depleted since there is almost no change in depletion depth and threshold voltage. In case the NHGATE device is turned off and reverse biased with $V_{BS} = -1\,\mathrm{V}$, the body-effect transconductance is in the range of $g_{mb} = 1 \cdot 10^{-11}\,\mathrm{S}$ and increases to $g_{mb} = 1 \cdot 10^{-9}\,\mathrm{S}$ at 400 °C.

Results for HGATE devices with a gate-source voltage of $|V_{GS1}| = 1\,\mathrm{V}$ in the range of the threshold voltage are shown in Figure 6.25 b). A larger body-effect transconductance can be seen when the gate-source voltage of the device is in the range of the threshold voltage as shown Figure 6.25 b). The values saturate at $g_{mb} = 1 \cdot 10^{-8}\,\mathrm{S}$ for all temperatures. A change of 10 mV on the body node of the device thereby results in a 100 pA change of drain current. Although the influence is small, RBB bias voltages need to be very stable and should provide low noise levels.

The body-effect transconductance of a PHGATE device is shown in Figures 6.26 a) and 6.26 b) for $V_{GS1} = 0\,\mathrm{V}$ and $V_{GS1} = -1\,\mathrm{V}$, respectively. Similar the the obtained results for the NHGATE device, the body effect transconductance is approximately $g_{mb} = 1 \cdot 10^{-11}\,\mathrm{S}$ at low temperatures but increases to $g_{mb} = 1 \cdot 10^{-9}\,\mathrm{S}$ at 400 °C. It can be seen from Figure 6.26 b) that the body-effect transconductance for PHGATE devices at threshold is also approximately $g_{mb} = 1 \cdot 10^{-8}\,\mathrm{S}$ and thereby similar to that of the NHGATE.

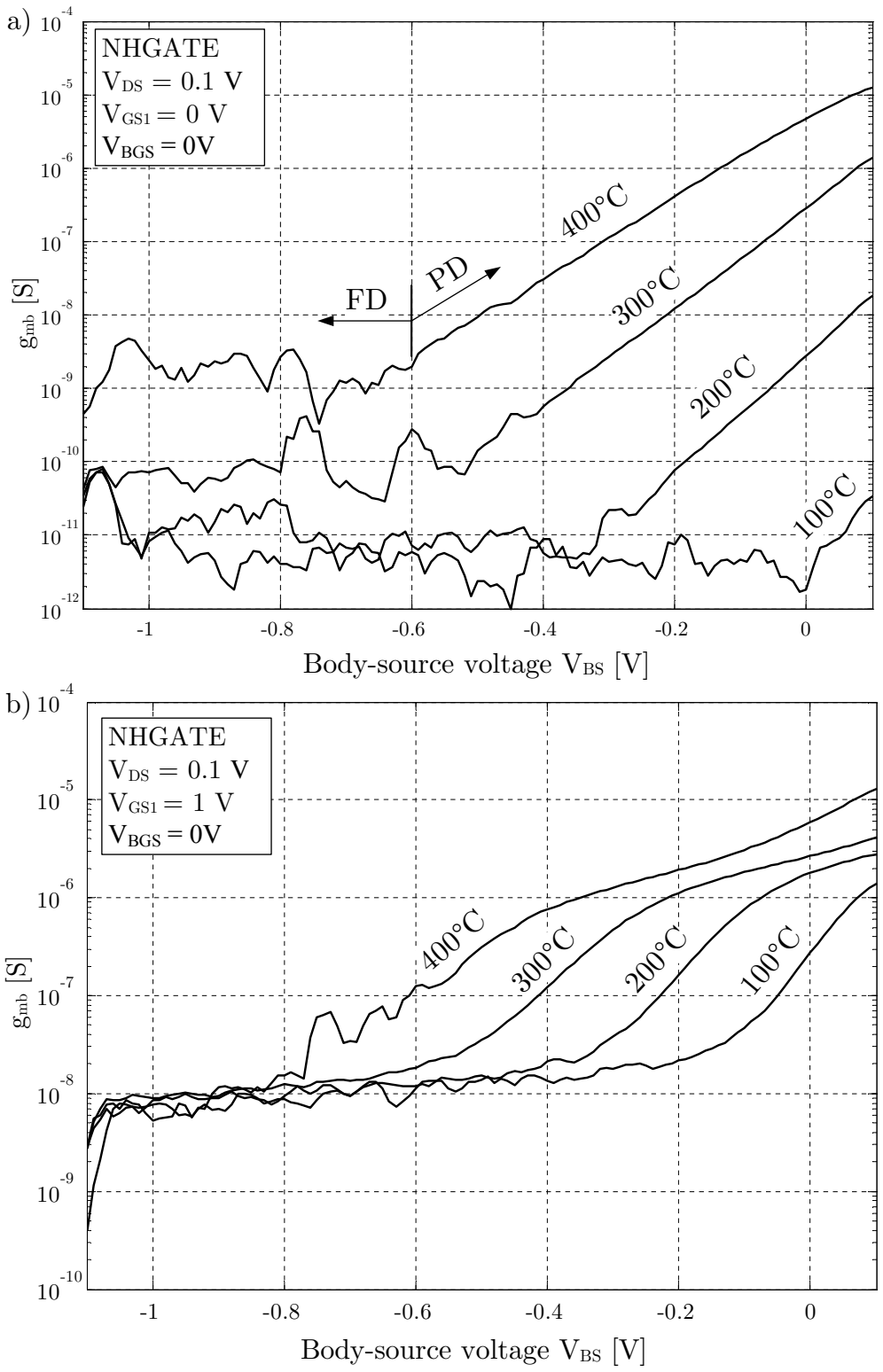

Figure 6.25: Body-Effect Transconductance g_{mb} of an NHGATE device over V_{BS} for different temperatures. a) with a gate-source voltage of $V_{GS1} = 0\,\mathrm{V}$. b) with a gate-source voltage of $V_{GS1} = 1\,\mathrm{V}$.

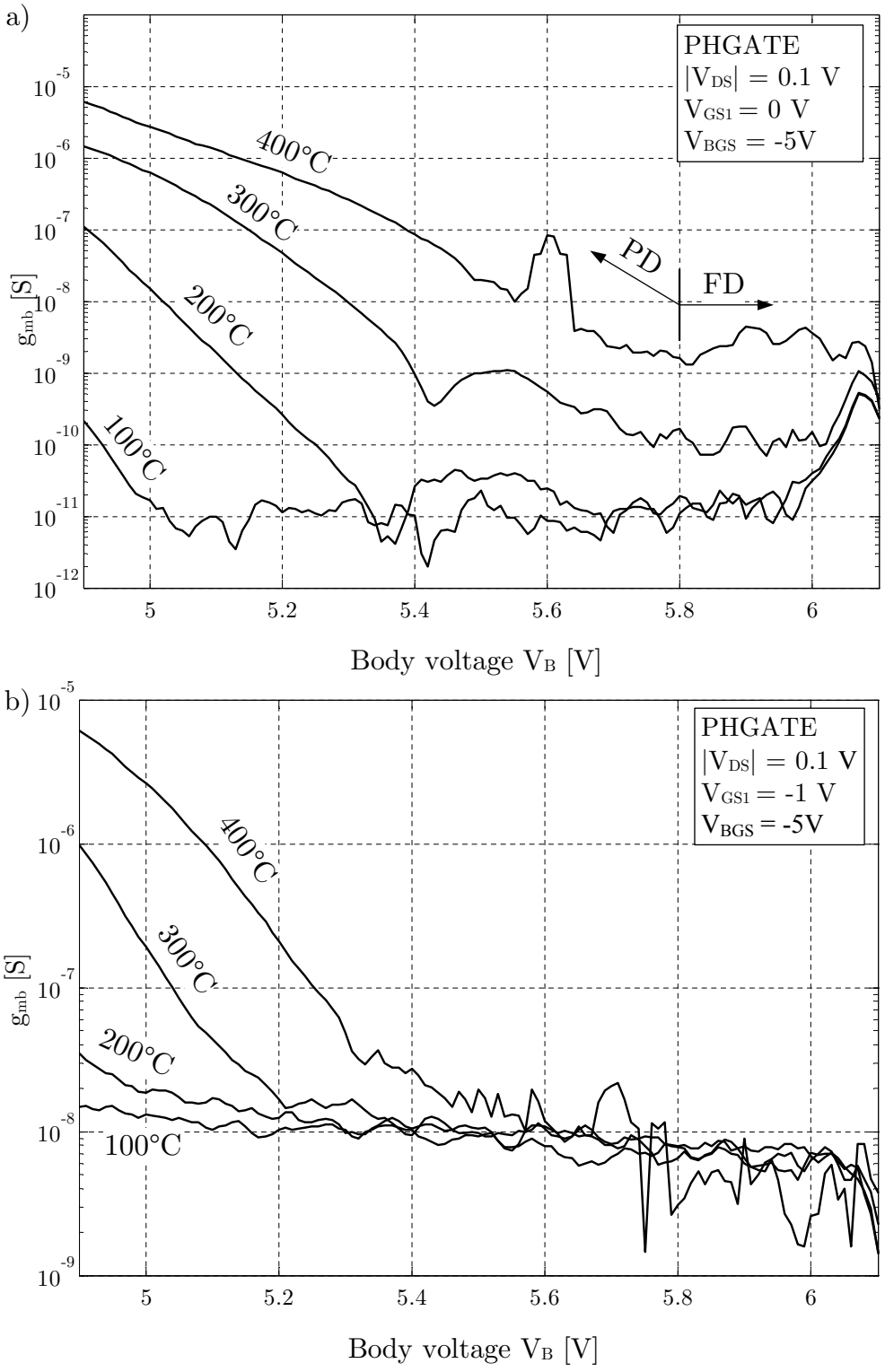

Figure 6.26: Body-Effect Transconductance g_{mb} of a PHGATE device over V_{BS} for different temperatures. a) with a gate-source voltage of $V_{GS1} = 0\,\mathrm{V}$. b) with a gate-source voltage of $V_{GS1} = -1\,\mathrm{V}$

6.17 Summary

It was shown in this chapter that elementary device characteristics such as the threshold voltage, leakage current level, transconductance efficiency factor g_m/I_d as well as intrinsic gain can be improved by the proposed technique of reverse body biasing. First of all, the extension of depletion depth at high temperatures leads to a transition from a partially depleted device to a fully depleted device. As a result, the threshold voltage of the device is increased significantly at higher temperatures. Also the temperature coefficient of the threshold voltage in FD mode is smaller compared to PD mode. Since the device is fully depleted up to 400 °C, the device's threshold voltage drops linearly in the considered temperature range. It was also shown that the front gate surface potential is affected by the influence of RBB. This effect leads to a decrease of the subthreshold leakage current, since the device does not enter weak inversion at high temperatures. The overall leakage current level thereby decreases about more than one order of magnitude over the entire temperature range. With reduced leakage currents also the I_{ON}/I_{OFF} ratio of both N-channel SOI-MOSFET devices and P-channel SOI-MOSFET devices improves by a factor of 100.

When the body of HAGTE devices is not short-circuited with source, the body-effect transconductance g_{mb} is larger than zero. A body-effect transconductance of approximately $g_{mb} = 1 \cdot 10^{-8}$ S was measured for NHGATE and PHGATE devices. A change of about 10 mV on the body node of the device thereby results in a change of 100 pA in drain current of the device. As this effect can decrease the overall gain, e.g. in NHGATE intrinsic gain stages where sources are not grounded, it has to be considered a drawback from the proposed technique. An investigation of the influence on intrinsic gain in more complex analog circuits is presented in the next chapter. It was also demonstrated that RBB significantly increases the g_m/I_d factor and thereby also the intrinsic gain of HGATE SOI-MOSFETs. The Early voltage at low drain-source voltages is slightly decreased when RBB is applied, which is also a drawback of RBB. The reduction almost vanishes at increased drain-source voltages, though. An important result at this point is that the Early voltages at high temperatures can still be determined for very low drain currents. Thereby, operation in the moderate inversion region of the devices is still possible up to 400 °C, which was inaccessible due to leakage currents without RBB.

In the next chapter, the proposed technique is investigated in terms of applicability to analog circuits. Beside a method to generate the required reverse bias signals, also the benefits for analog circuitry need to be analyzed. Further it

will be demonstrated, how RBB improves the circuit performance of basic analog circuits which were presented in Chapter 5.

Chapter 7

Application of Reverse Body Biasing in Analog Circuits

The analog characteristics of SOI-MOSFETs at high temperatures were discussed in detail in Chapter 4. The impact on analog circuits resulting from the degradation of SOI-MOSFET characteristics were also presented in Chapter 5. It was shown that leakage currents lead to increased errors and also cause malfunctions in analog circuits at very high temperatures. It was also demonstrated that fully depleted SOI-MOSFET devices have a much better high temperature operation capability compared to partially depleted SOI-MOSFET devices. As it was shown in the previous chapter, a PD SOI-MOSFET device can be turned into a FD SOI-MOSFET device without modification of the SOI process when the required minimum reverse bias voltage is applied. Improved analog characteristics of fully depleted SOI-MOSFET devices are thereby available in a partially depleted SOI technology.

RBB requires the generation of additional bias voltages. In case the SOI-MOSFET devices are operated within the voltage supply rails from $V_{GNDA} = 0\,\mathrm{V}$ to V_{DDA}, the required RBB voltages need to be lower than V_{GNDA} and higher than V_{DDA} for N-channel devices and P-channel devices, respectively. Methods to generate the on-chip RBB potentials outside the voltage supply rails of the chip are discussed in this section. In addition, circuit design techniques to apply RBB to analog circuits within the supply voltage rails, based on shifted source potentials are investigated from a theoretical point of view. In order to keep the general applicability of the presented approach, basic analog circuits, e.g. common source-, common drain- and common gate gain stages are discussed in detail. Experimental results of the investigated circuits with the use of RBB at high temperatures are presented afterwards. The results are compared to the

prior obtained results from Section 5 in order to prove the improvement of analog circuits with the use of RBB.

7.1 Generation of On-Chip RBB Voltages

Analog circuits are operated within the voltage supply rails from V_{GNDA} to V_{DDA}. In the considered SOI technology, the positive supply voltage V_{DDA} is 5 V. In order to keep the full signal swing, the reverse body biasing voltages V_{BN} and V_{BP} need to be lower and higher than V_{GNDA} and V_{DDA}, respectively. The minimum reverse bias voltages for NHGATEs and PHGATEs were defined in Section 6.3. The required RBB voltages within analog circuits are then given in Equations (7.1) and (7.2), respectively.

$$V_{BN} = V_{GNDA} - V_{BNmin} \tag{7.1}$$

$$V_{BP} = V_{DDA} + V_{BPmin} \tag{7.2}$$

The required minimum reverse bias voltages for NHAGTE and PHGATE SOI-MOSFET devices up to 400 °C were determined to be approximately 0.5 V for both devices. This results in reverse bias voltages of $V_{BN} = -0.5\,\text{V}$ and $V_{BP} = 5.5\,\text{V}$ for NHGATEs and PHGATEs, respectively. One considerable approach for the generation of the bias voltages is the implementation of a dual supply charge pump, as presented in [KMB+08]. Additional external storage capacitors may be required to store sufficient charge for the reverse biasing of many devices at the same time. A draw-back of this technique is the amount of additional circuity, required to realize the charge pumping circuits. Another drawback is the resulting voltage ripple on V_{BN} and V_{BP}, which is induced by the clocking of the charge pump circuit. As V_{BN} and V_{BP} are directly connected to the film of the SOI-MOSFET devices, any disturbance results in a modulation of the drain-source current of the connected SOI-MOSFET devices. It was shown in Figure 6.16 that the body-effect transconductance of fully depleted SOI-MOSFETs at threshold is approximately $g_{mb} = 1 \cdot 10^{-8}\,\text{S}$, also at high temperatures. A voltage ripple of 10 mV then results in a drain-source current change of 1 nA. This solution may therefore not be suitable for low noise applications. At this point further work is necessary to realize a suitable bias voltage generation method.

7.2 RBB through Shifted Source Potential

In case RBB voltages cannot easily be generated on-chip and also external RBB voltages cannot be provided, RBB can also be realized by the variation of the source potential of SOI-MOSFET devices. For example, when the film of an NHGATE device is connected to ground, a negative V_{BS} is achieved by increasing the source potential of the NHGATE device. Unfortunately, the increased source potential results in a higher minimum output voltage, and thereby in decreased signal swing. Nevertheless, in some cases this technique may provide the applicability of RBB without the effort of on-chip RBB voltage generation. In the following sections, fundamental analog circuits are analyzed in order to determine the resulting signal swing, which is required for the reverse biasing of the devices within the supply voltage rails.

7.2.1 Analog Switch

The high temperature characteristics of analog switch was demonstrated in Section 5.1.1. Experimental results were obtained in order to investigate the overall leakage current of the analog switch at high temperatures. An off-state leakage current of approximately 2 µA was measured at 400 °C. It was also shown that the dominating part of the overall leakage current in P-channel and N-channel SOI-MOSFET devices is the subthreshold leakage current. In this section, the leakage behavior of the analog switch with the use of RBB is investigated in detail. A schematic view of the analog switch is shown in Figure 7.1 a). Charge injection compensation structures are neglected to simplify the analysis.

Figure 7.1 a) also shows the parasitic body-source and body-drain PN-junction diodes of the SOI-MOSFETs. This visualization was chosen to better distinguish between the PN-junction leakage current and the subthreshold leakage current in the following analysis. The only currents flowing from drain to source in the depicted SOI-MOSFET devices are the subthreshold currents. When the switch is turned off, the resulting leakage current I_L at the output node is given by

$$\begin{aligned} I_L &= I_{SUB} + (I_{PN-P} - I_{PN-N}) \\ &= (I_{SUB-N} + I_{SUB-P}) + (I_{PN-P} - I_{PN-N}) \ . \end{aligned} \tag{7.3}$$

The subthreshold leakage currents of both MOSFET devices are the dominating portion of the overall leakage current I_L. With the use of RBB, the

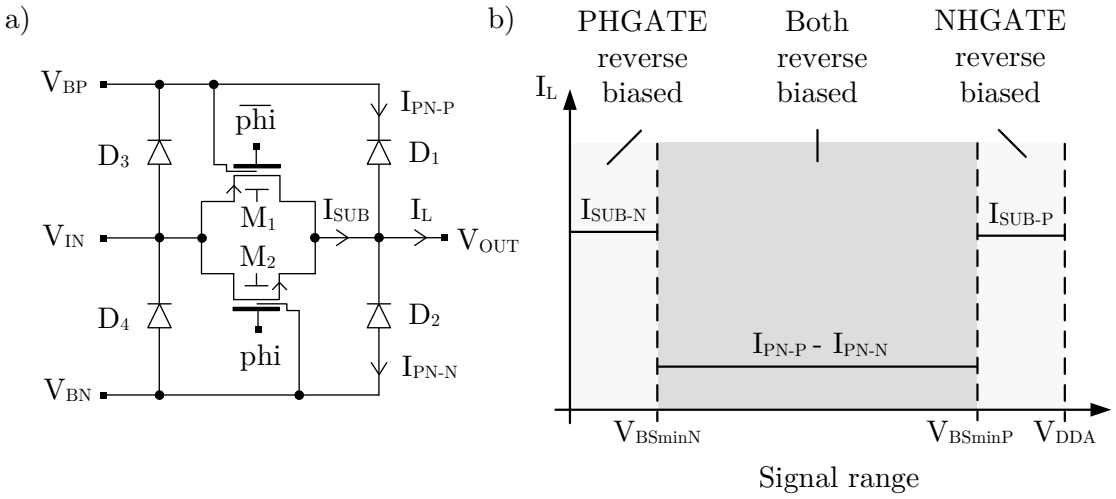

Figure 7.1: a) Schematic view of a symmetrical analog switch composed of HGATE SOI-MOSFET devices including their parasitic PN-junction diodes. b) Qualitative leakage current over signal range.

subthreshold leakage current can be effectively eliminated, as it was shown in Section 6.8.

Figure 7.1 b) shows the signal range, i.e. the absolute voltage levels of V_{IN} and V_{OUT}, for which both SOI-MOSFET devices are reverse biased with the minimum reverse bias voltage V_{BSmin}. Drain and source of both devices are determined by the levels of V_{IN} and V_{OUT}. For the following consideration, the film of M_1 is connected to the positive supply voltage (V_{BP}=V_{DDA}) and the body terminal of M_2 is connected to ground ($V_{BN} = 0\,\mathrm{V}$). If $V_{IN} > V_{OUT}$, the source and drain terminals of both devices are determined as shown in Figure 7.1 a). In this case, the source of M_1 is connected to V_{IN}. The device is reverse biased for input voltages lower than $V_{DDA} - V_{BSminP}$, whereby V_{BSminP} is approximately 0.5 V in the considered SOI technology. The source of the N-channel SOI-MOSFET device M_2 is connected to V_{OUT}. M_2 is reverse biased in case V_{OUT} is higher than V_{BSminN}. The input- and output voltage range, in which both devices are reverse biased reaches from V_{BSminN} up to ($V_{DDA} - V_{BSminP}$). Within this voltage range, only the PN-junction leakage currents of the parasitic PN-junction diodes D_1 and D_2 contribute to the overall leakage current I_L. In this case, only the difference of both PN-junction currents remains.

$$I_L = I_{PN-P} - I_{PN-N} \tag{7.4}$$

The voltage across D_1 is given by

$$V_{D1} = V_{BP} - V_{OUT} = V_{DDA} - V_{OUT} \tag{7.5}$$

and the voltage across D_2 is given by

$$V_{D2} = V_{OUT} - V_{BN} = V_{OUT} \, . \tag{7.6}$$

The voltages across the diodes are complementary, which would result in an opposite modulation of the PN-junction leakage currents. Since the switch is symmetrical, the example above is also valid for the case $V_{IN} < V_{OUT}$. With applied RBB, the devices remain fully depleted, as demonstrated before. Thereby, the modulation of the PN-junction depletion volume by an applied drain-source voltage is much smaller compared to partially depleted devices. In case the depletion volumes of both devices match, the resulting PN-junction currents cancel each other out, which results in a very low overall leakage current.

The reverse biasing voltages V_{BP} and V_{BN} have to meet the following requirements:

$$V_{BN} = min\left(V_{IN}, V_{OUT}\right) - V_{BSminN} \tag{7.7}$$

$$V_{BP} = max\left(V_{IN}, V_{OUT}\right) + V_{BSminP} \tag{7.8}$$

The reverse biasing of the analog switch within the supply voltage rails is thereby feasible, when the minimum reverse bias voltages V_{BSminN} and V_{BSminP} are considered as the minimum and maximum voltages of the signal. Whether these additional constraints are acceptable, has to be evaluated individually for a specific application.

7.2.2 Current Mirrors

Current mirrors are essential analog building blocks used in operational amplifiers, voltage references or to provide bias currents for various chip components. The high temperature capability of a basic current mirror was demonstrated in Section 5.1.2. It was shown that increased temperatures lead to significant errors. The errors are caused by leakage currents inside the SOI-MOSFET devices in case the operating current is in the range of the leakage currents level. As good matching is usually essential for current mirrors, large device widths are required and leakage currents thereby increase. The operation of the current mirror with very low

operating currents below 1 µA is critical as leakage currents can easily exceed the operating current level.

Reverse biasing of the current mirror can be realized by the implementation of an additional source resistance in the input- and output path of the current mirror. In this case, the degenerated source effect leads to increased output resistance of the current mirror. A schematic of the NHGATE current mirror and additional source resistors R_S is illustrated in Figure 7.2.

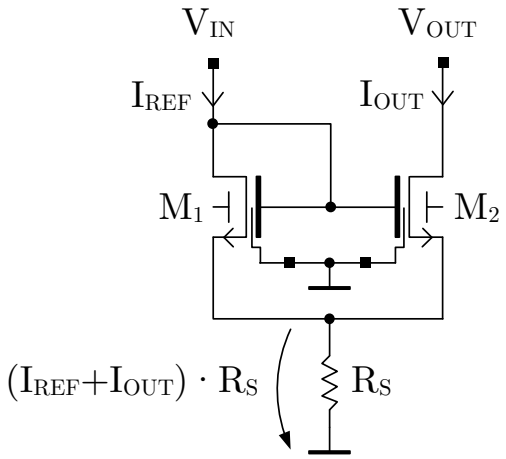

Figure 7.2: Basic current mirror with degenerated source.

The additional source resistor R_S increases the source potential of both devices to $(I_{REF} + I_{OUT}) \cdot R_S$. When the film of both devices is grounded, the effective reverse bias for both devices results in

$$V_{BS1,2} = -\left(I_{REF} + I_{OUT}\right) \cdot R_S \; . \tag{7.9}$$

The output resistance of the degenerated source current mirror including the body effect is given by (7.12) [Raz10].

$$r_{out} = r_{ds2}\left[1 + R_S\left(g_{m2} + g_{mb2}\right)\right] + R_S \tag{7.10}$$

The small-signal body-effect transconductance g_{mb} can be written as shown in Equation (7.11) [Raz10].

$$g_{mb2} = (n-1)\, g_{m2} \tag{7.11}$$

Using Equation (7.11), the resulting output resistance of the current mirror can be simplified to

$$r_{out} = r_{ds2}\,(1 + g_{m2} n R_S) + R_S\ . \tag{7.12}$$

It can be seen from Equation (7.12) that the body effect, as well as the additional source resistors increase the output resistance of the current mirror. One drawback of the technique is the increased minimum output voltage of the current mirror. The minimum output voltage of the current mirror with degenerated source results is the sum of the saturation voltage of M_2 and the voltage drop across R_S, given by

$$V_{OUTmin} = V_{Dsat2} + R_S \cdot (I_{REF} + I_{OUT}) \tag{7.13}$$

Large source resistances are required for very small reference currents. The source resistor R_S is therefore more likely implemented using the channel resistance of an SOI-MOSFET transistor. Techniques to further decrease the minimum output voltage of the current mirror using more advanced topologies are well known and are not within the focus of this work. Although additional effort is necessary to implement an effective reverse bias in these more advanced current mirrors, the presented current mirror is an example to realize RBB in current mirror topologies.

7.2.3 Common Source Amplifier Stage

Basic single stage amplifiers are widely used in analog circuit design. More complex amplifiers like two stage operational amplifiers or transconductance amplifiers consist of single or cascaded basic gain stages. The investigation of these basic gain stages regarding the applicability of RBB thereby also provides the basics of more complex amplifier circuits, which are not discussed in details here. The intrinsic gain of basic analog gain stages, i.e. common source, common drain and common gate stages is investigated in this section using small-signal analysis.

The common source amplifier is often used as an inverting stage in operational amplifiers like in the two stage op-amp, which was shown in Chapter 5. Figures 7.3 a) and b) show an NHGATE SOI-MOSFET common source amplifier stage including a source resistance R_S and the corresponding small signal equivalent circuit, respectively [Raz10].

It has to be mentioned at this point that a source resistance can also occur by an increased ground resistance due to the resistance of metal lines. For the following analysis, the film of the NHGATE is considered grounded. Two cases have to be considered in the analysis of the common source stage: One, in which

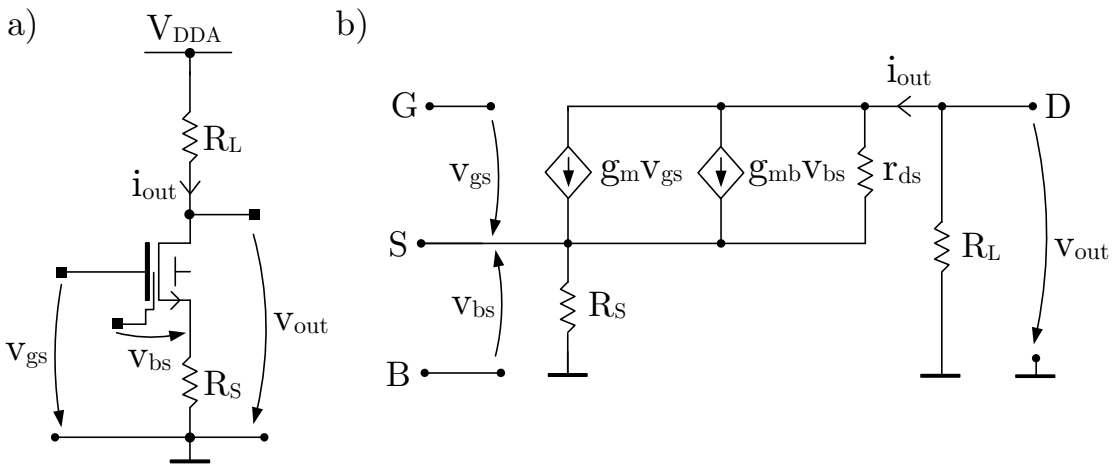

Figure 7.3: a) NHGATE SOI-MOSFET common source amplifier stage. b) Small signal equivalent circuit of a).

$R_S = 0$ and one, in which $R_S > 0$. In case R_S is equal to zero, the body-effect can be neglected since the body-source small signal voltage is also zero. In case $R_S > 0$, degeneration of the common source gain stage can occur [Raz10]. In this case, v_{bs} is non-zero and modulated by the gate-source small signal voltage v_{gs}. Including the body-effect, the resulting voltage gain of the degenerated common source stage is given by (7.14) [Raz10].

$$A = \frac{v_{out}}{v_{gs}} = \frac{-g_m r_{ds} R_L}{r_{ds}\left[1 + (g_m + g_{mb})\, R_S\right] + R_L + R_S} \tag{7.14}$$

Equation (7.14) can be simplified using Equation (7.11). The gain of the common source stage then results in

$$A = \frac{v_{out}}{v_{gs}} = \frac{-g_m r_{ds} R_L}{r_{ds}\left(1 + n g_m R_S\right) + R_L + R_S}\,. \tag{7.15}$$

The overall degradation due to the body-effect is almost negligible since n is very small for reverse biased fully depleted SOI-MOSFETs. When RBB is applied to the common source gain stage, i.e. the body-effect is considered, there is also an increase in output resistance as given in Equation (7.16) [Raz10].

$$R_{out} = r_{ds}\left(1 + n g_m R_S\right) + R_S \tag{7.16}$$

In summary, the resulting effects of RBB on the common source gain stage are quite small, since the SOI-MOSFET device is fully depleted. In case of a partially depleted device, the body factor can reach much higher values at high temperatures, which results in a much stronger degradation effect compared to the

fully depleted case. Similar to the example of the current mirror, RBB can only be realized when the minimum reverse bias voltage V_{BSmin} is considered. Thereby, also the minimum output voltage of the common source stage is increased. The reverse biasing of the common source stage without degenerated source effect and thus reduced output swing, requires additional work.

7.2.4 Common Drain Amplifier Stage

Common drain gain stages can be used as voltage buffers as they are able to provide high output currents and low output resistance. Figures 7.4 a) and b) show the common drain stage and the corresponding small signal equivalent circuit, respectively [Raz10].

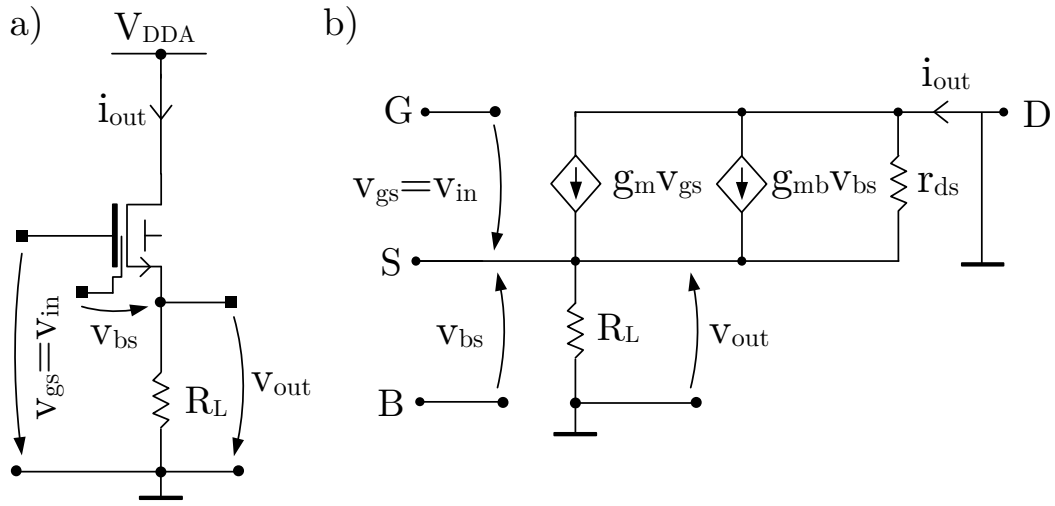

Figure 7.4: a) NHGATE SOI-MOSFET common drain amplifier stage. b) Small signal equivalent circuit of a).

The voltage gain of a common drain gain stage, or source follower, is given in Equation (7.17) [Raz10].

$$A = \frac{v_{out}}{v_{in}} = \frac{g_m R_L}{1 + R_L\,(g_m + g_{mb})} = \frac{g_m R_L}{1 + n g_m R_L} \tag{7.17}$$

As it can be seen from Equation (7.17), the voltage gain is smaller than 1 and is further reduced by the body factor n. Without body effect, n is replaced by 1. Only a small degradation of A is observed when n is set to 1.09 for a fully depleted SOI-MOSFET. As a positive effect, the body effect reduces the output resistance of the common drain stage, which is given in Equation (7.18) [Raz10].

$$R_{out} = r_{ds} \,||\, \frac{1}{g_m} \,||\, \frac{1}{g_{mb}} \tag{7.18}$$

Since g_{mb} is small in fully depleted state, the reduction of the output resistance is expected to be very low. In case the film of the HGATE SOI-MOSFET is connected to ground, the body-source DC voltage is given by $V_{BS} = -V_{OUT}$. The minimum output voltage, for which the device is effectively reverse biased is defined by

$$V_{OUTmin} = V_{BSminN} \ . \tag{7.19}$$

In the considered SOI technology at 400 °C, V_{BSminN} is approximately 0.5 V, as it was shown in Figure 6.3. Thus, reverse bias is effectively applied to the common drain stage for output voltages higher than 0.5 V. The required input voltage V_{IN} is then given by

$$V_{INmin} = V_{th} + V_{BSminN} \ . \tag{7.20}$$

In summary, it can be seen that the gain of the common drain stage reduces by a small amount when RBB is applied. In contrary, the output resistance also decreases by a small amount. Both effect are small in case the SOI-MOSFET devices are fully depleted. The common drain stage can be reverse biased quite easily in case the minimum input voltage is higher than V_{INmin} given in (7.20).

7.2.5 Common Gate Amplifier Stage

Common gate stages are very often used as cascodes to increase the output resistance of a common source amplifier stage. The common gate stage with resistive load R_L and its small signal equivalent circuit are shown in Figures 7.5 a) and b), respectively.

Neglecting the body-effect ($g_{mb} = 0$), the gain of the common gate stage loaded with a resistor R_L is given in (7.21) [Raz10].

$$A = \frac{v_{out}}{v_{in}} \approx g_m \left(r_{ds} || R_L\right) \tag{7.21}$$

When the film of the device is grounded, the small-signal body-source voltage is given by $v_{bs} = -v_{in}$. The gain increases due to the small-signal transconductance g_{mb} as shown in Equation (7.22) [Raz10].

$$A = \frac{v_{out}}{v_{in}} \approx \left(g_m + g_{mb}\right) \left(r_{ds} || R_L\right) \approx n g_m \left(r_{ds} || R_L\right) \tag{7.22}$$

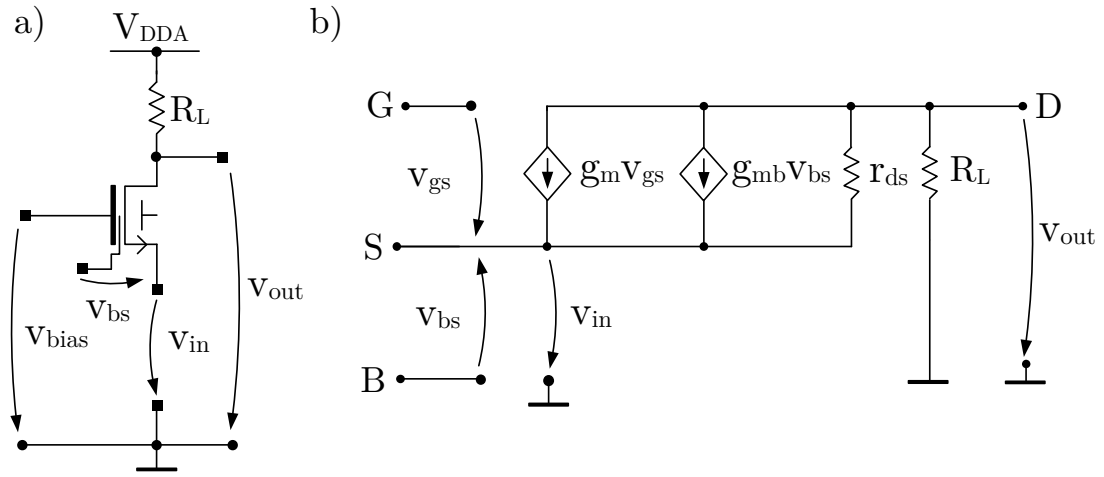

Figure 7.5: a) NHGATE SOI-MOSFET common gate amplifier stage. b) Small signal equivalent circuit of a).

In this case, n is 1.09 for reverse biased, fully depleted SOI-MOSFET devices. Reverse bias of the common gate can be achieved for $V_{IN} > V_{BSmin}$.

7.2.6 Two-stage Operational Amplifier

It was demonstrated in Section 5.1.3 that the operating point of moderate inversion of the two-stage operational amplifier's gain stages is critical for high temperature operation. The open loop DC gain dramatically reduces at high temperatures, as it was shown in Figure 5.11 in Section 5.1.3 due to leakage currents in both gain stages. Nevertheless, moderate inversion is an optimal operating point for both gain stages to reach adequate gain values for high gain applications. Since all devices are more likely operated in strong inversion for high bandwidth applications, device sizes are small and the operating current level is much higher than the leakage current level. As a result, high bandwidth applications are not as much affected as applications where high gain is required. High gain applications remain a challenge at high temperatures and require additional effort. The input- and output signal range of the amplifier for the realization of RBB within the voltage supply rails is described in the following sections. A schematic of the operational amplifier circuit is depicted in Figure 7.6.

For the operation of the first gain stage, the input differential pair M_3 and M_4 as well as M_2 need to be operated in saturation. The minimum common mode input voltage is given by

$$V_{CMmin} = V_{th3,4} + V_{Dsat2} \; . \tag{7.23}$$

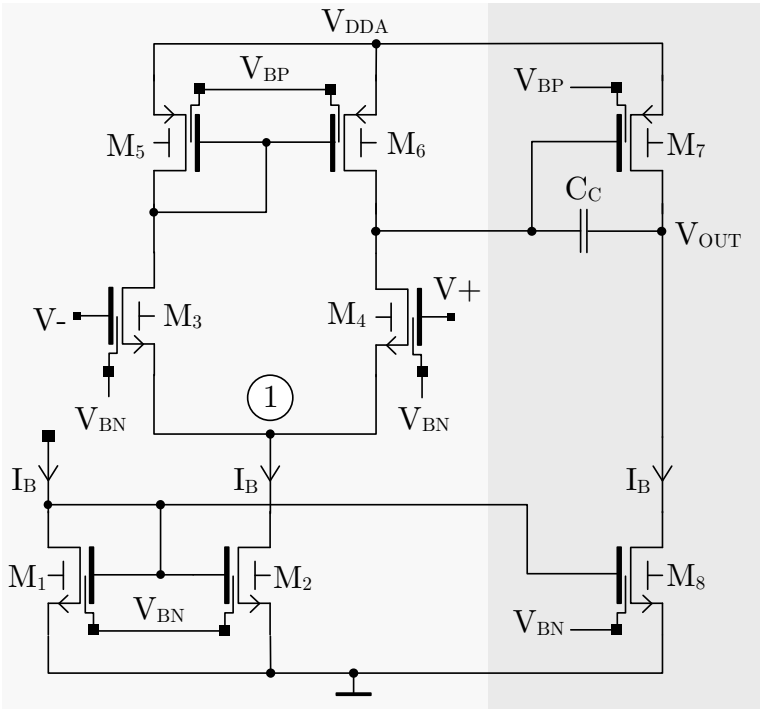

Figure 7.6: Two-stage operational amplifier using HGATE SOI-MOSFETs.

If the common mode operating voltage V_{CM} is further increased, the potential at node 1 follows V_{CM} minus the threshold voltage $V_{th3,4}$.

$$V_1 = V_{CM} - V_{th3,4} \tag{7.24}$$

In case the film terminals of the differential input stage transistors are connected to ground ($V_{BN} = 0\,\mathrm{V}$), the effective reverse bias of the differential stage devices M_3 and M_4 is given by

$$V_{BS3,4} = -V_1 = V_{th3,4} - V_{CM}\ . \tag{7.25}$$

A reverse bias of V_{BSminN} is required for the full depletion of the differential input stage. It is important to mention here that both devices also exhibit a back-gate effect, which lowers the required reverse bias voltage due to depletion at the back-interface of the silicon film. Nevertheless, the back-gate effect is neglected in this analysis. The minimum common mode input voltage, to keep the input stage fully depleted is given by

$$V_{CMmin} = V_{th3,4} + \max\left(V_{BSminN}, V_{DSat2}\right)\ . \tag{7.26}$$

In case $V_{BSminN} > V_{DSat2}$, the minimum common mode input voltage to ensure proper RBB decreases by $V_{BSminN} - V_{Dsat2}$.

For differential input signals, node 1 can be considered a virtual ground node and is thereby grounded for the small signal analysis of the first stage [Raz10]. In this case, the first stage represents a common source stage without source resistance [Raz10]. By setting $R_S = 0$ in Equation (7.15) from Section 7.2.3, the gain of the common source stage is given by

$$A|_{R_S=0} = -g_{m4} r_{ds4} || r_{ds6} \ . \tag{7.27}$$

For the common mode small signal analysis, the first gain stage can be considered a common source stage with r_{ds2} being the source small signal source resistance. The gain of the differential pair is then given by [Raz10]

$$A_{CM} = \frac{-g_{m4} r_{ds4} r_{ds6}}{r_{ds4} \left[1 + n g_{m4} r_{ds2}\right] + \frac{1}{2} r_{ds6} + r_{ds2}} \ . \tag{7.28}$$

By increasing the output resistance of the current mirror r_{ds2}, the common mode rejection can be increased significantly. In addition, the body effect of the reverse biased differential stage is supporting the rejection of common mode signals.

The reverse biasing of the N-channel current mirror consisting of the devices M_1, M_2 and M_8, can be realized with the use of an source resistance, as described in Section 7.2.2. Thereby, also an increased output resistance can be achieved, which is beneficial for the rejection of common mode signals. The drawback at this point is the increase of the minimum common mode input voltage of the input stage, i.e. the decreased input swing.

Reverse biasing of the second stage is more challenging since the implementation of an additional resistance at the source of M_7 directly affects the output swing and also reduces the gain of the stage due to the degenerated source effect. At this point, a circuit concept is required, which offers the possibility to bias the source of M_7 at $V_{S7} = V_{DDA} - V_{BSminP}$. The drawback again is the decreased output swing of the gain stage, which is then limited to $V_{OUTmax} = V_{DDA} - V_{BSminP} - V_{Dsat7}$.

Reverse body biasing of the the two-stage operational amplifier within the supply rails can be achieved at the cost of decreased input- and output swing. In case the considered application does not allow this limitation, the bias voltages must be below and above V_{GNDA} and V_{DDA} for NHGATEs and PHGATEs, respectively.

7.3 Experimental Results

In this section, RBB is applied experimentally at high temperatures in order to demonstrate the resulting effect on analog circuits. Measurements are taken in a high temperature oven. The bias voltages V_{BN} and V_{BP} were applied externally using an external voltage source. The entire measurement setup is described in appendix A.2. Basic analog circuits, which were already discussed in Chapter 5 are investigated below with the use of RBB.

7.3.1 Analog Switch

The analog switch including charge injection compensation structures is shown in Figure 7.7.

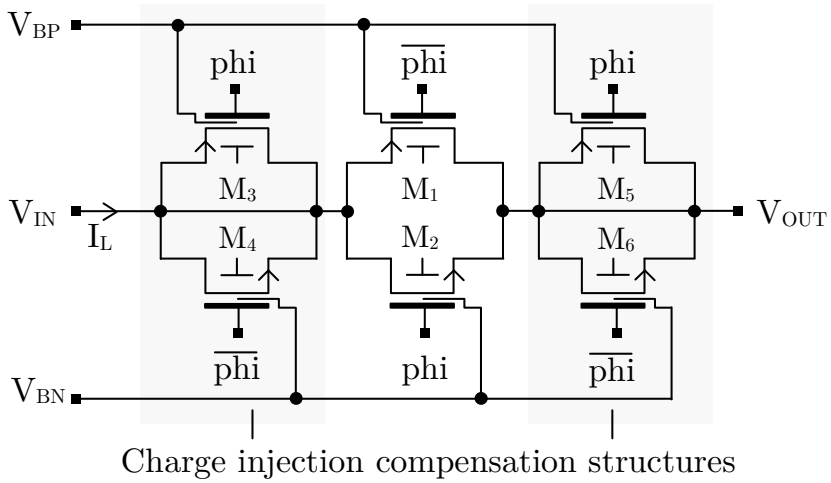

Figure 7.7: Schematic view of a symmetrical analog switch composed of HGATE SOI-MOSFET devices including charge injection compensation structures.

The input- and output signal range of the switch is 0 V to 5 V. For the following investigation, the input voltage is $V_{IN} = 5\,\mathrm{V}$ whereby the output voltage V_{OUT} is grounded. In this configuration, it is expected that both devices M_1 and M_2 are non-reverse biased and the sum of both subthreshold leakage currents is measured at the output node of the switch.

It is important to mention here that charge injection compensation structures also add a PN-junction leakage current portion to the overall leakage current. In case RBB is applied, the body biasing voltages of NHGATEs and PHGATEs are set to $V_{BN} = -1\,\mathrm{V}$ and $V_{BP} = 6\,\mathrm{V}$, respectively. Figure 7.8 presents experimental results of the leakage current over temperature when the switch is turned off with and without applied RBB.

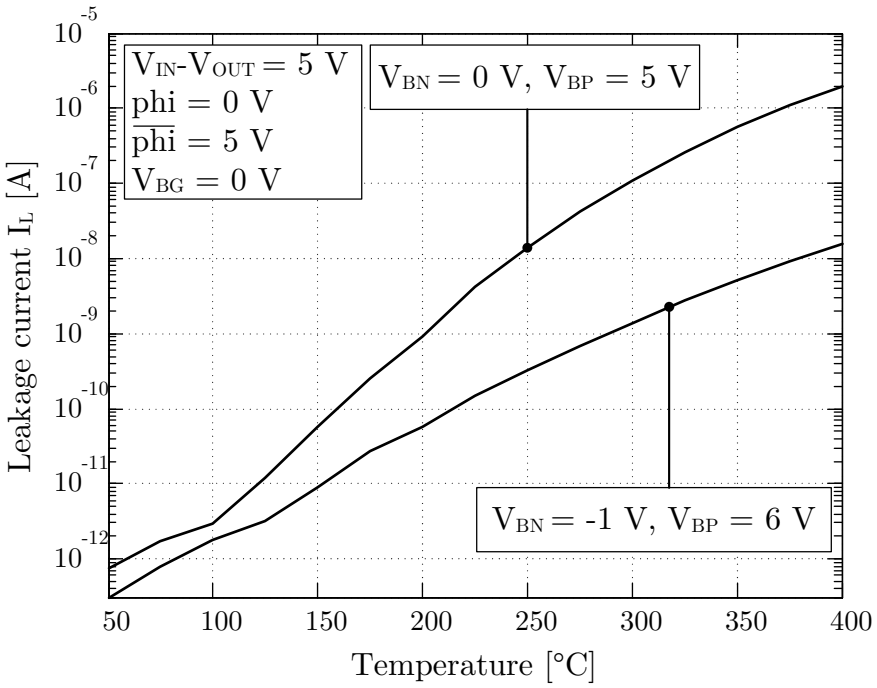

Figure 7.8: Experimental results of the overall leakage current I_L with and without applied RBB.

The overall leakage current at 400 °C is reduced by almost two orders of magnitude, i.e. from 2 µA down to 16 nA. These results demonstrate the effective leakage current reduction when RBB is applied to the switch. In Section 5.1.1, the error which results from a leakage current of 2 µA with a 20 pF capacitor over a time period of 10 µs was calculated to be approximately 1 V. When RBB is applied, this error reduces to

$$\Delta V_C|_{RBB} = \frac{\Delta Q}{C_1} = \frac{I_L \Delta t}{C_1} = \frac{16\,\text{nA} \cdot 10\,\mu\text{s}}{20\,\text{pF}} = 8\,\text{mV}\ . \tag{7.29}$$

The resulting error $\Delta V_C|_{RBB}$ is reduced by a factor of 125 when RBB is applied to the circuit. Nevertheless, the obtained results show a significant reduction of the analog switch's leakage currents at high temperatures. Due to lower leakage currents, switches capacitor circuits are able to run at lower operating speeds. As a result, the bandwidth of operational transconductance amplifiers can be reduced. The DC open loop gain can be increased instead, which improves the overall accuracy of switched capacitor circuitry.

7.3.2 Current Mirrors

Basic N-channel and P-channel SOI-MOSFET current mirrors are investigated in this section with the use of RBB and compared to the results obtained from

the non-biased current mirrors. Reverse bias voltages were applied externally. A schematic view of the investigated current mirrors are shown in Figures 7.9 a) and b) for the N-channel and the P-channel SOI-MOSFET current mirror, respectively.

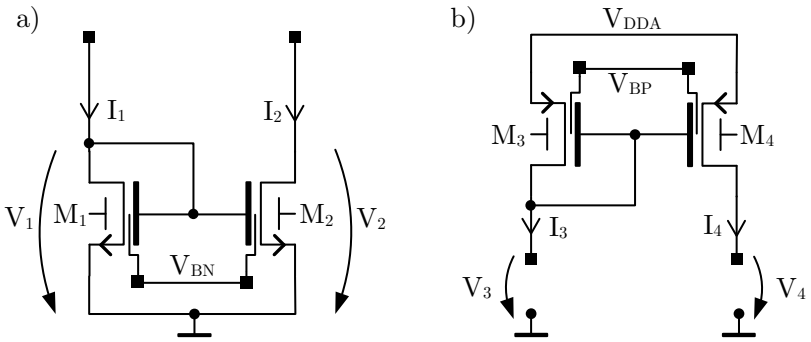

Figure 7.9: Basic current mirror using RBB a) N-channel SOI-MOSFETs and b) P-channel SOI-MOSFETs.

A bias current of $I_1 = I_3 = 100\,\text{nA}$ is injected in both current mirrors. The investigation of the current mirror at very low biasing currents is especially useful for low power circuits or superior order temperature compensation in bandgap reference circuits. Within this application, current mirrors are used to inject very small correction currents into the output path of the bandgap reference circuit. Superior order temperature compensation techniques thereby rely on the precision of current mirrors at very low biasing currents and high temperatures. Figures 7.10 a) and b) show the previous obtained results from section 5.1.2 and Figures 7.10 c) and d) show results for the basic current mirrors with applied RBB.

Comparing the overall percentage error for the NHAGTE in Figures 7.10 b) and d), it can be seen that the error reduces significantly when RBB is applied, especially at high temperatures. The error decreases down to 4.5 % at 350 °C and down to 41 % at 400 °C.

Experimental results for the PHGATE current mirror, consisting of the devices M_3 and M_4, are shown in Figures 7.11 a-d). It can be seen that the use of RBB reduces the overall error of PHGATE current mirrors from 93 % down to 8.6 % at 350 °C and from 455 % down to 11.5 % at 400 °C.

7.3.3 Two-stage Operational Amplifier

In this section, the open loop DC gain of the basic two-stage operational amplifier is experimentally investigated up to 400 °C using RBB. The measurements were carried out using a network analyzer with a DC offset of V_{CM} at the positive input. The common mode operating point is $V_{CM} = V_{DDA}/2$. The output of the

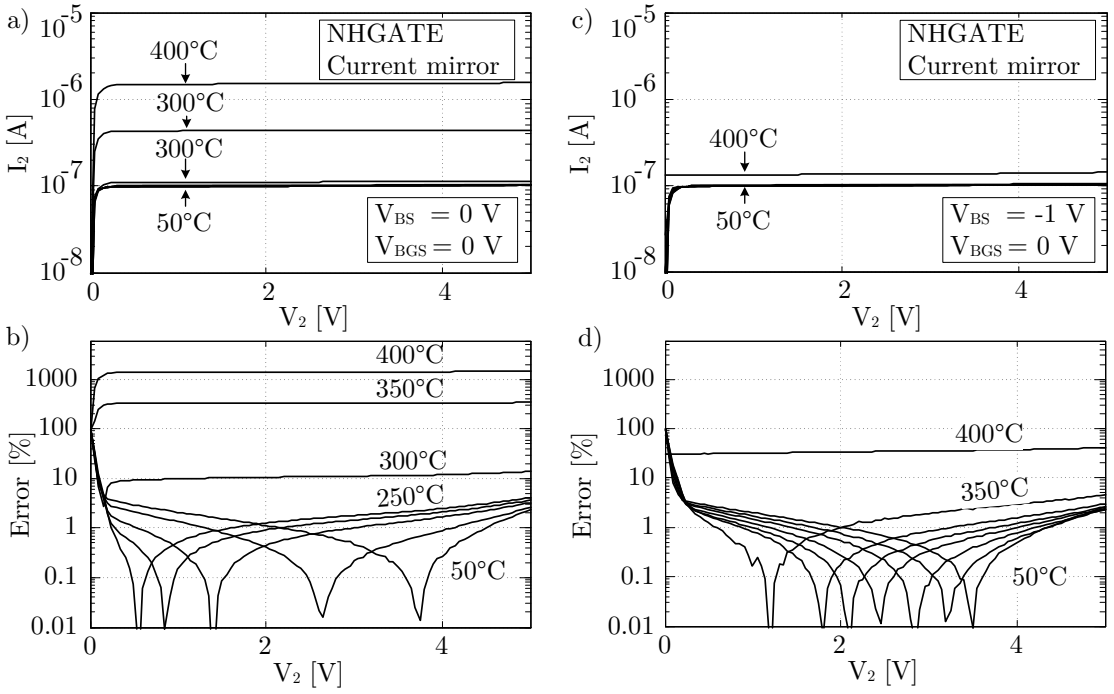

Figure 7.10: Output current of the NHGATE current mirror a) without RBB b) error without RBB c) with applied RBB d) error with applied RBB.

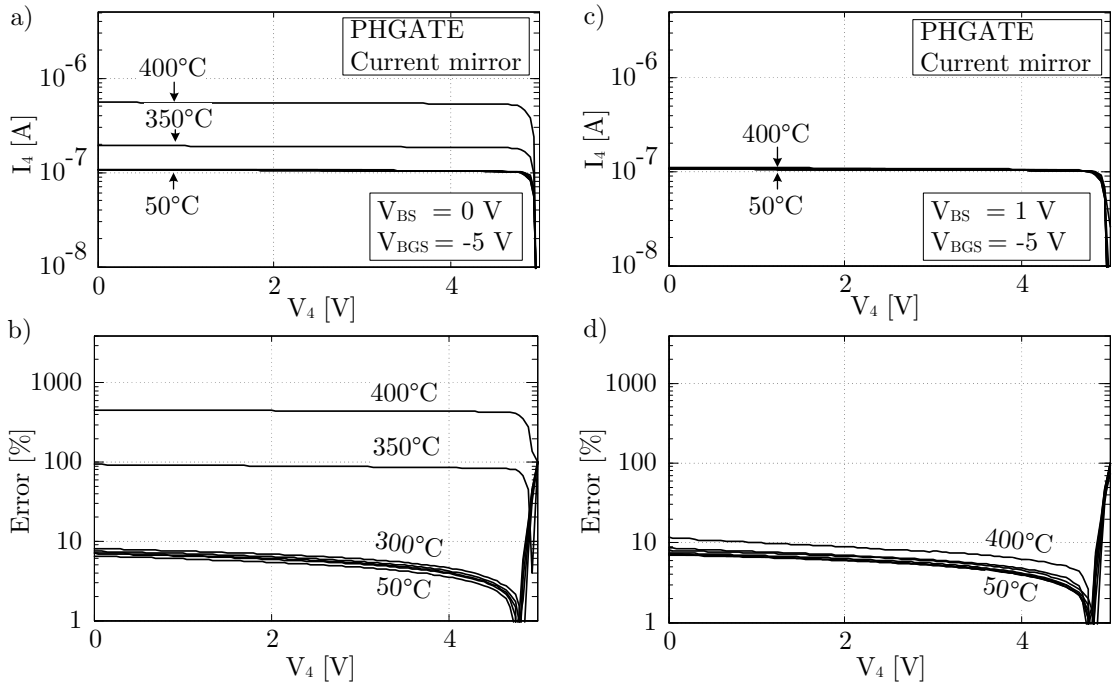

Figure 7.11: Output current of the PHGATE current mirror a) without RBB b) error without RBB c) with applied RBB d) error with applied RBB.

amplifier was buffered by an external wideband J-FET amplifier. The influence of the J-FET amplifier was eliminated by calibration of the signal path to decouple the load of the network analyzer. All channel lengths are 4.8 µm. The bias current I_B is mirrored equally into the first and second stage. For a bias current of $I_B = 3.3\,\mu A$ and a W/L ratio of 16, the transistors M_3, M_4 and M_7 operate in the mid moderate inversion region. All other devices operate in strong inversion. Measurement results are presented in Figure 7.12 [SKK13b].

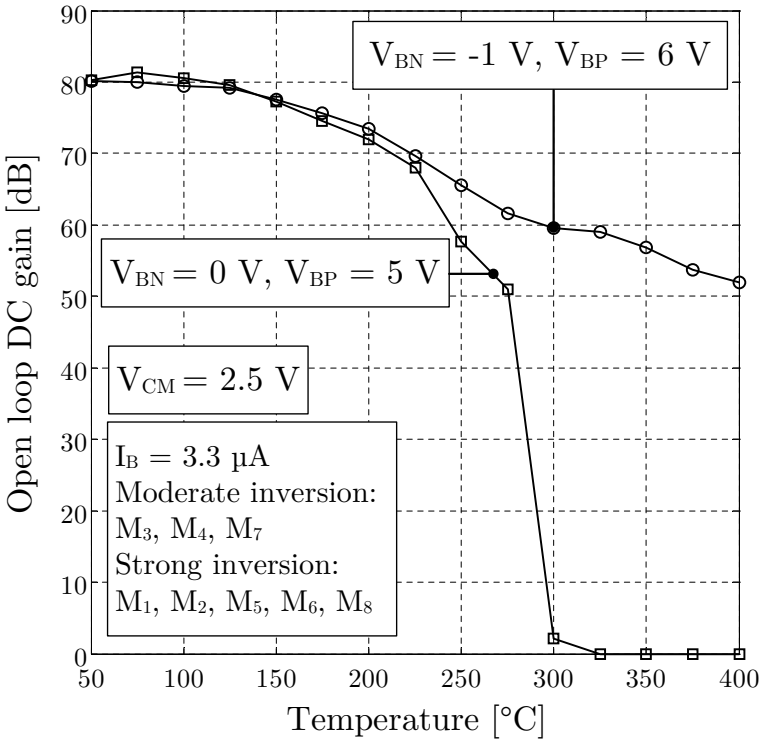

Figure 7.12: Open loop DC gain of a two-stage op-amp with and without applied RBB.

Without RBB, the DC gain of the amplifier decreases starting from around 225 °C. With applied RBB, an open loop DC gain of 52 dB can still be achieved at 400 °C. Due to the high common mode input voltage, it is expected that the differential stage is also reverse biased and thereby fully depleted in the non-reverse-biased case ($V_{BN} = 0\,V$). Since the differential stage is fully depleted, whether RBB is used or not at high input common mode voltages, the enhanced high temperature performance of the op-amp can be related to the reverse biasing of the second gain stage only. External reverse biasing of the first gain stage with $V_{BN} = V_{BSminN}$ also ensures operation at very low common mode input voltages. In contrary, reverse biasing of the output stage is required in the entire common mode voltage range.

In summary, it was demonstrated that the high temperature operating capability of a two-stage operation amplifier is greatly enhanced when RBB is applied to the circuit. Nevertheless, RBB has to be realized at the loss of input- and output voltage swing of the amplifier if reverse biasing outside the voltage supply rails cannot be provided externally.

7.3.4 Bandgap Voltage Reference

A bandgap circuit is a widely used voltage reference, also for high temperature applications. The high temperature operating capability was investigated in Section 5.1.4. It was found that the reference output voltage is affected by low threshold voltages and increased leakage currents. Thus, proper circuit operation at high temperatures remains a challenge [GDS+12]. RBB is implemented in order to improve high temperature operation of the bandgap reference circuit. The first order bandgap circuit demonstrated in Section 5.1.4 is now shown in Figure 7.13 using HGATE devices.

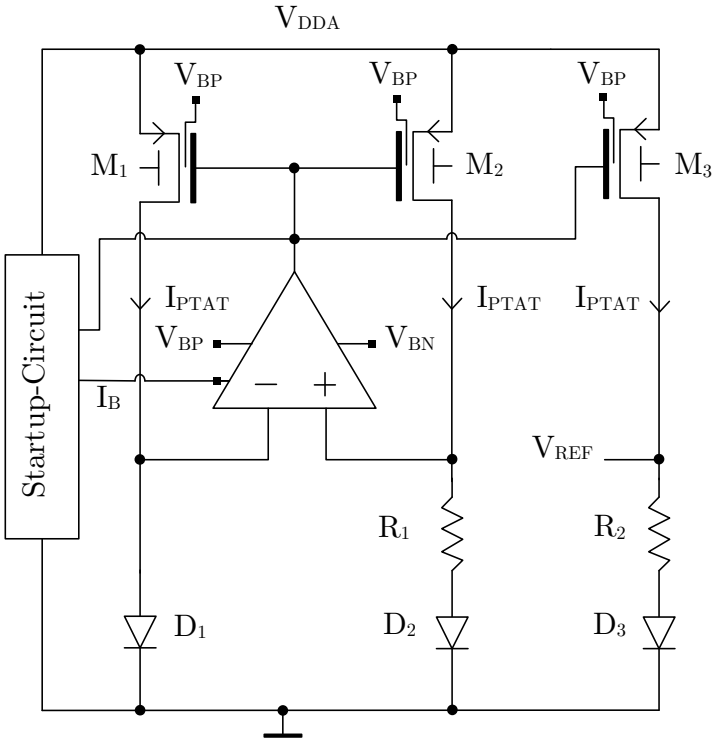

Figure 7.13: Bandgap voltage reference using NHGATE SOI-MOSFET devices.

RBB is applied externally for the PHAGTE current sources M_1-M_3 and the operational amplifier. The two-stage operational amplifier discussed in the last section was implemented using reverse biasing of both gain stages. Measurement

results of the bandgap voltage reference with and without applied RBB are shown in Figure 7.14 [SKK13a].

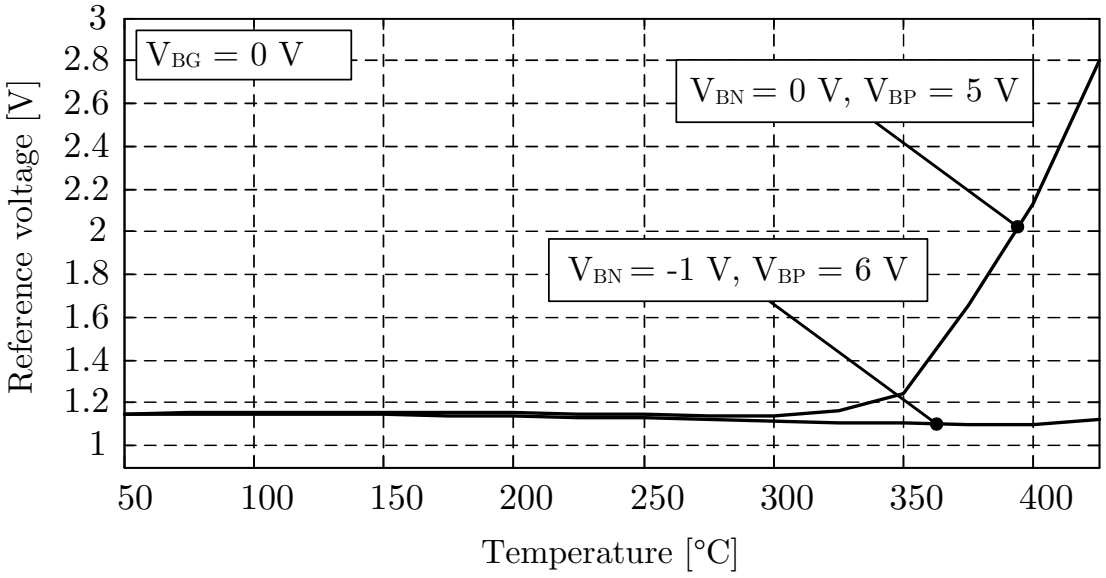

Figure 7.14: Measured Bandgap reference voltage with applied RBB ($V_{BN} = -1\,\mathrm{V}$; $V_{BP} = 6\,\mathrm{V}$) and without ($V_{BN} = 0\,\mathrm{V}$; $V_{BP} = 5\,\mathrm{V}$) applied RBB.

It can be seen that the operating temperature range of the bandgap reference is extended up to 425 °C when RBB is applied to the circuit. Two effects enable the operation of the reverse biased bandgap reference up to 425 °C. First of all, the threshold voltages $V_{thM1-M3}$ of the current source devices $M_1 - M_3$ do not get close to 0 V when RBB is applied. The output voltage of the operational amplifier, which is needed in order to bias the current source devices at threshold, is thereby kept within the upper output voltage swing of the amplifier. As a second effect, the amplifier itself does support sufficient gain up to 425 °C, which is the result of leakage current reduction inside the op-amp, as discussed in the previous section. RBB significantly improves the circuit performance of advanced voltage references up to 425 °C, as it can be seen from these experimental results.

7.4 SOI-MOSFET Model for Circuit Simulation

To simulate SOI-MOSFET devices, the BSIMSOI device model is typically used. Although this work focuses on experimental results, the availability of simulation models is an important aspect for the study of RBB in analog circuits. Especially the transition from fully to partially depleted at high temperatures needs to be

considered in circuit simulation. The BSIMSOI simulation model distinguishes between partially depleted (`soimod=0`), fully depleted (`soimod=2`) and a unified SOI depletion model (`soimod=1`) [BSI03]. As it is stated in [PFW+03b] and [PFW+03a], the existence of a built-in potential lowering ΔV_{bi} is the most relevant difference between partially depleted SOI-MOSFETs and fully depleted SOI-MOSFETs and is therefore used in the BSIMSOI device model. The built-in potential lowering ΔV_{bi} was already discussed in Section 3.5.2 and its first order approximation was given in Equation (3.50). It is once again written in Equation (7.30) [PFW+03a].

$$\Delta V_{bi} = \phi_{S1} - \frac{qN_{CH}t_{SI}^2}{2\epsilon_{si}} \tag{7.30}$$

This expression is used for first order approximations in this work, whereby a more detailed form of Equation (3.49) is used in the BSIMSOI simulation model [BSI03]. Since the model parameter for the channel doping concentration `Nch` and the film thickness `Tsi` are used to determine ΔV_{bi}, these model parameters cannot easily be used as fitting parameters during device model extraction. In addition, also the first order body effect coefficient K_1, the front gate oxide thickness `Tox` and the back gate oxide thickness `Tbox` need to match real process dimensions. The leakage current level of the SOI-MOSFET device has to be adjusted with the parameters `Isrec` and `Isbjt`. The subthreshold slope needs to be adjusted using `Nfactor`. In case the subthreshold slope and leakage currents cannot be matched to the obtained measurement results, it may be required to use two device models, one for the RBB case and one for the non-biased case. It has to be mentioned at this point that proper device model extraction is necessary in order to fit both cases, non-biased and reverse biases, into one simulation model.

7.5 Summary

A first approach for the application of RBB in basic analog circuits was demonstrated in this chapter. RBB voltages need to be generated on-chip or have to be provided externally. The generation of RBB on-chip voltages still remains a challenge and further investigations are necessary at this point. Nevertheless, if the film of NHGATE and PHGATE devices is connected to the supply voltage rails, RBB can also be realized with the drawback of decreased signal voltage swing. To demonstrate the resulting effect of RBB on basic analog circuits, RBB was applied externally and measurement results of an analog switch, current mirrors, an operational amplifier and a bandgap circuit at high temperatures were

presented. In summary, it was shown that the high temperature operation of the investigated analog circuits is significantly enhanced when RBB is applied to the circuits.

Chapter 8

Conclusion

8.1 Summary and Key Findings

The presented work investigates the influence of reverse body biasing (RBB) on fundamental SOI-MOSFET device characteristics and analog circuits at high temperatures, fabricated in a PD-SOI technology. Temperature limitations of the studied SOI technology were derived from the silicon film thickness and the doping concentrations and are in good agreement with experimentally obtained results. It is concluded that operation within the intrinsic region of silicon is possible but requires the consideration of high leakage currents, which affect the operation of analog and digital circuits.

In this work, SOI-MOSFET devices with an H-shaped gate were investigated in the Fraunhofer IMS 1.0 µm PD-SOI technology. These devices provide a separate body-contact and are therefore suitable for the realization of reverse body biasing. It was found that these devices remain fully depleted up to considered temperature of 400 °C when RBB is applied. The non-linear decrease of the device's threshold voltage at high temperatures can be effectively reduced. Threshold voltages of 800 mV and −350 mV are achieved by applying RBB to N-channel and P-channel HGATE SOI-MOSFETs respectively at 400 °C. The subthreshold leakage current is the dominating portion of the overall leakage current at high temperatures. A fully depleted silicon film also results in improved subthreshold slope characteristics and thereby reduced subthreshold leakage currents at high temperatures. As a result, SOI-MOSFET device leakage currents are reduced by more than one order of magnitude. The I_{ON}/I_{OFF} ratio of reverse biased SOI-MOSFET devices is increased by a factor of 40 compared to the non-biased case.

In addition, the g_m/I_d factor is improved significantly, especially in the moderate inversion region. By applying RBB, SOI-MOSFET devices are able to operate in the mid moderate inversion region, while achieving intrinsic gain values of 54.4 dB at 400 °C, compared to 40.2 dB without RBB. Due to the operation in moderate inversion, the intrinsic gain is increased by more than 14 dB per device. The intrinsic bandwidth is increased by a factor of approximately 2.7 . . . 4.7, as the depletion state of the device is changed from partially depleted to fully depleted when RBB is applied. Table 8.1 shows an overview of the experimental results obtained in this work.

Table 8.1: Comparison of NHGATE SOI-MOSFET device characteristics with applied RBB and without RBB at 400 °C.

Characteristics at 400 °C	without RBB $V_{BS} = 0\,\mathrm{V}$	with applied RBB $V_{BS} = -1\,\mathrm{V}$
V_{th}	0.15 V	0.8 V
$\partial V_{th}/\partial T$	$\approx -2\,\mathrm{mV/°C}$	$-0.75\,\mathrm{mV/°C}$
S	$510\,\mathrm{mV}/dec$	$146\,\mathrm{mV}/dec$
I_{ON}/I_{OFF}	$2 \cdot 10^2$	$8 \cdot 10^3$
$I_{OFF}/(W/L)$ @ $V_{GS} = 0\,\mathrm{V}$	300 nA	18 nA
g_m/I_d	$0.8\,\mathrm{V}^{-1}$ @ $I_d/(W/L) = 1.5\,\mu\mathrm{A}$	$10\,\mathrm{V}^{-1}$ @ $I_d/(W/L) = 100\,\mathrm{nA}$
A_i	40.2 dB @ $I_d = 5.5\,\mu\mathrm{A}$	54.4 dB @ $I_d = 200\,\mathrm{nA}$

As one can see, the use of reverse body biasing significantly improves the high temperature characteristics of PD-SOI MOSFET devices.

A comparison of the high temperature capability of state of the art integrated device technologies is presented in Table 8.2. State of the art body tied (BT) PD-SOI devices, FD-SOI devices with a film thickness of 30 . . . 80 nm, UTB-FD devices with a film thickness of 7 nm and FinFET devices are compared to the results obtained in this work. The results are compared at a temperature of 250 °C since experimental results in the stated technologies up to 400 °C are not provided.

Table 8.2: Comparison of SOI-MOSFET device characteristics in different SOI technologies at 250 °C.

Characteristics	PD-SOI RBB $t_{SI} = 150\,\text{nm}$ (this work)	BT PD-SOI $t_{SI} = 150\,\text{nm}$ [ETVJR08]	FD-SOI $t_{SI} = 30 \ldots 80\,\text{nm}$	UTB FD-SOI $t_{SI} = 7\,\text{nm}$ [KAFF11]	FinFET
$\partial V_{th}/\partial T$	$-0.75\,\text{mV/°C}$	$-0.7\,\text{mV/°C}$ **	$-0.7\,\text{mV/°C}$ [FAA+01] $-0.57\,\text{mV/°C}$ [VKD+03] $\approx -0.4\,\text{mV/°C}$ [ZCS+07] $-0.5\,\text{mV/°C}$ [KVMF05]	$-0.63\,\text{mV/°C}$	$-0.8\,\text{mV/°C}$ [TPM+08] $-0.6\,\text{mV/°C}$ [MWC+06] $-0.6\,\text{mV/°C}$ [AMS+07]
S @ 250 °C	146 mV/dec	160 mV/dec	125 mV/dec [ZCS+07]* 150 mV/dec [RKC+02]	115 mV/dec	120 mV/dec [AMS+07]* 150 mV/dec [TPM+08]
I_{ON}/I_{OFF} @ 250 °C	$2 \cdot 10^6$	888 ***	$6 \cdot 10^3$ [FAA+01]	$2 \cdot 10^4$	-
$I_{OFF}/\mu\text{m}$ @ 250 °C	0.08 nA	$\approx 800\,\text{nA}$	0.5 nA [FAA+01] 0.5 nA [VKD+03]	28 nA	0.5 nA/per fin [KVMF05]
g_m/I_d @250 °C $I_d = 100\,\text{nA}$	$10\,\text{V}^{-1}$	-	$10\,\text{V}^{-1}$ [FAA+01]	-	-

* Values have been extrapolated up to 250 °C
** Due to high channel doping $N_{CH} = 1 \cdot 10^{18} cm^{-3}$. Typical value for PD-SOI: $-2\,\text{mV/°C}$
*** Low threshold voltage of $\approx 200\,\text{mV}$ causes high leakage currents at 250 °C

In this work, the threshold voltage temperature coefficient of reverse biased PD-SOI MOSFET devices is in the same range as the values obtained in other works for BT PD-SOI, FD-SOI, UTB FD-SOI and FinFET devices. At this point it should be mentioned that BT PD-SOI usually exhibit a threshold voltage temperature coefficient of around $-2\,\mathrm{mV/°C}$. In the work of [ETVJR08], the low threshold voltage coefficient is achieved using a high channel doping concentration of $N_{CH} = 1 \cdot 10^{18} cm^{-3}$. UTB FD-SOI and FinFET devices show slightly lower values of subthreshold swing compared to the results obtained this work. The I_{ON}/I_{OFF} ratio achieved with RBB is significantly higher compared to the other technologies, which results from a high threshold voltage with decreased leakage currents if RBB is applied. The g_m/I_d values of reverse biased PD-SOI MOSFET devices, investigated at an operating current of 100 nA are comparable to the values obtained for FD-SOI MOSFET devices. In summary, these results show that RBB is a useful method to improve the high temperature characteristics of PD-SOI MOSFET devices and also to achieve results comparable to those of FD-SOI MOSFET devices.

Reverse biasing requires some additional effort, i.e. the generation of body bias potentials outside the supply rails of the circuit in order to reach full signal swing. A circuit design approach to bias the devices within the supply voltage range is presented and evaluated for basic analog circuit components. Reverse biasing is thereby possible at the cost of reduced signal swing. Further work may concentrate on methods to extend the analog voltage swing.

It was also demonstrated, how basic analog circuits, e.g. an analog switch, basic current mirrors, a two-stage operational amplifier and a first order bandgap voltage reference are affected by increased operating temperatures. Analog switches suffer from high leakage currents at high temperatures. Within switched capacitor circuits for example, these leakage currents result in errors, which affect the circuit's accuracy. Increased errors in basic current mirrors do not allow the use of current mirrors for low current applications below 1 µA, e.g. for superior order temperature compensated voltage references. Also operational amplifiers, which are designed to achieve high DC open loop gain values are significantly affected by increased operating temperatures. These operational amplifiers cease operation at high temperatures as device leakage currents reach the level of operating currents. It was also demonstrated that the first order bandgap voltage reference, which utilizes current mirrors and an operational amplifier is significantly affected by decreased threshold voltages and increased leakage currents at high temperatures up to 400 °C.

Reverse body biasing was applied to these basic analog building blocks and experimental results were compared to the non-biased circuits. It was found that the high temperature operating capability of these circuits is improved significantly when RBB is applied. The reduction of leakage currents in analog switches, error reduction in current mirrors, sufficient open loop gain of operational amplifiers and a temperature stable reference voltage are the results obtained when RBB is applied at high temperatures. These results not only prove the enhancement of analog SOI-MOSFET device characteristics using RBB at high temperatures, they also demonstrate the resulting impact on fundamental analog circuits for high temperature applications.

8.2 Outlook and Future Work

In this work, reverse body biasing was investigated in a 1.0 µm PD-SOI technology. As technology developments pursue the downsizing of device channel lengths, it is of great interest, how reverse body biasing can be effectively applied to next generation high temperature SOI technologies. Analog circuits in smaller technology nodes are also more likely realized utilizing long channel devices, since long channel devices show a much better analog performance compared to short channel devices. Nevertheless, the influence of short-channel effects (SCE) on the effectiveness of RBB has to be considered if channel lengths are decreased. The effectiveness of RBB in upcoming technology nodes is estimated by the investigation of the minimum reverse body biasing voltage as a function of doping concentration and silicon film thickness. The minimum reverse bias voltage increases with increased doping concentration and decreases when the silicon film thickness is reduced. Using the same film thickness and higher doping concentrations in smaller technology nodes requires higher reverse body biasing voltages. The requirements for the realization of RBB in these technologies should be focused by future research activities in this field. The transition from fully depletion to partially depletion is also present in state of the art FinFET devices and depends on the fin width [RTK+06]. As a matter of fact, partially depleted device characteristics may also occur in FinFET devices at high temperatures [AMS+07]. The influence of RBB on the high temperature device characteristics of body-contacted FinFET devices should therefore also be investigated in future work.

Furthermore, all results in this work were obtained by carrying out short term high temperature measurements. Additional long term measurements are required

in order to analyze the effects of RBB on the reliability of analog circuits at high temperatures. Since thick insulating gate oxides were used within the considered high temperature, high voltage technology, the investigation of the reliability has not been within the focus of this work. Finally, the presented approach for the application of RBB in analog circuits should be further developed in future work. Also the use of the adaptive body biasing (ABB) technique within PD-SOI analog circuits at high temperatures should be further investigated.

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Appendix A

Material and Measuring Methods

Measuring techniques as well as type and origin of the materials investigated in this work are described here. All measurements were carried out on SOI wafers or separate dies in a chip package, processed at the Fraunhofer IMS fabrication site in Duisburg, Germany. In order to obtain the results presented in this work, SOI devices and circuits were experimentally investigated using different measurement setups, which are described in A.2, A.3 and A.4.

A.1 Material

SOI-MOSFET devices and circuits, fabricated in the Fraunhofer IMS 1.0 µm SOI CMOS technology were investigated in this work. The technology features 3 layers of tungsten metalization. Different batches and wafers were investigated, whereby the wafers were qualified for measurements by post-fabrication measurements. Silicon film thickness, threshold voltage, leakage currents, capacitances, etc. were determined for each wafer. All selected material represents *typical corner* material within the specifications of the considered SOI technology. The investigated SOI-MOSFET devices and circuits were measured in a ceramic DIL28 die package. Aluminum and conducting silver glass solder were used for wire-bonding and die-attachment, respectively.

A.2 High Temperature Oven

An industrial high temperature oven was used in order to achieve high temperature DC measurement result. The oven was used for SOI-MOSFET device characterization measurements, which are presented in Chapters 4 and 6. All small signal parameters of SOI-MOSFET devices were obtained from DC measurements. The

oven was also used to obtain measurement results for the analog switch, basic current mirrors and the bandgap voltage reference presented in Sections 5 and 7.

A ceramic chip package heater setup was used for the investigation of the open loop DC gain of the operational amplifiers. Since AC signals were required for these measurements, low capacitive signal paths were provided. The ceramic chip-heater setup is described in detail in Section A.4.

The exact model designation of the oven used in this setup is KU70/06/A from THERMCONCEPT Dr. Fischer GmbH & Co. KG. The oven is capable of reaching a maximum temperature of 600 °C, whereby 425 °C was the upper temperature in this work. A PID-controller, named *HtIndustry* by HTH8 s.r.o., is used to regulate the temperature inside the oven. The temperature accuracy of the controller is stated to be ±0.1 % in the temperature range up to 600 °C [HTH03]. Measurement was started after a hold time of 15 min after a certain temperature was reached. It was verified that this time period is sufficient for the temperature to reach the silicon die within the package. Small errors in effective junction temperature cannot be totally excluded, but are, as all comparative measurements were taken with the same method, of minor relevance to the results obtained in this work.

DIL28 die packages were used in a ceramic socket with spring contacts. High temperature cables (600 °C) were attached to the ceramic socket also using spring contacts. All high temperature cables were fed through a hole on the side of the oven in order to contact the chip-socket inside. Figure A.1 shows the entire measurement setup.

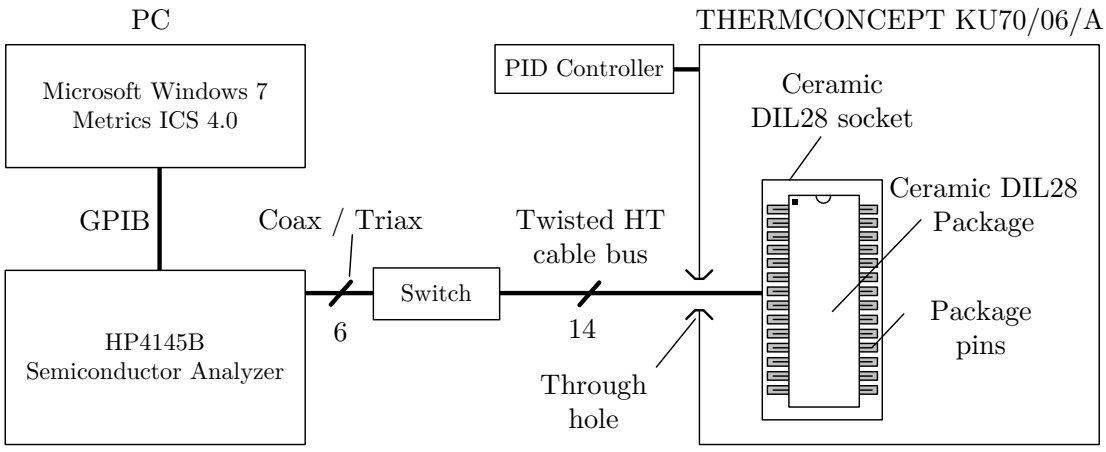

Figure A.1: High temperature oven measurement setup used for DC measurements of SOI-MOSFET devices and circuits.

The high temperature cable bus was twisted in order to reduce external disturbances. Since a power of 8 kW is necessary to operate the oven, and switching of the controller does occur during measurement, signal noise cannot be fully removed and is visible in some results at very low currents. Nevertheless, the generated noise does only affect measurements in the current range below 1 pA. A printed circuit board (PCB) was used to route the high temperature cables to the BNC connectors of the semiconductor analyzer. In this setup, the HP4154B semiconductor analyzer was used for all measurements. The analyzer was connected to a PC, running on Windows 7[1], using GPIB (IEEE-488) and is controlled by ICS[2] v4.0. All obtained data was exported to Microsoft Excel[3] and evaluated using MATLAB[4] v7.0.4. The MATLAB evaluation code, i.e. an example for an N-channel SOI-MOSFETs is given and described in detail in appendix B.

A.3 Wafer Prober with Thermo Chuck

A wafer prober with thermo chuck was used in order to carry out the measurement of device currents in Section 6.10. The measurement setup is equipped with high temperature probes and has a maximum operating temperature of 300 °C. The high temperature probes are connected to a HP4154B semiconductor analyzer using triax/coax cables. The semiconductor analyzer is connected to a PC via GPIB and controlled using Metrics ICS, as already described in appendix A.2.

A.4 Ceramic Chip-Package Heater

A ceramic chip-package heater was used for measurements of the operational amplifier investigated in Sections 5.1.3 and 7.2.6. The op-amp was assembled in a DIL28 ceramic chip package which is connected to a ceramic socket. The socket was mounted to a soldered circuit board. The ceramic heater was attached on top of the die package, so only the chip and the ceramic socket are directly exposed to high temperatures. High temperature solder was used for the connections on the backside of the circuit board. Figure A.2 a) and b) show the measurement setup and a closeup of the chip, respectively.

[1] WINDOWS is a registered trademark of the Microsoft Corporation.
[2] ICS is a registered trademark of Metrics Technology, Inc.
[3] EXCEL is a registered trademark of the Microsoft Corporation.
[4] MATLAB is a registered trademark of The MathWorks, Inc.

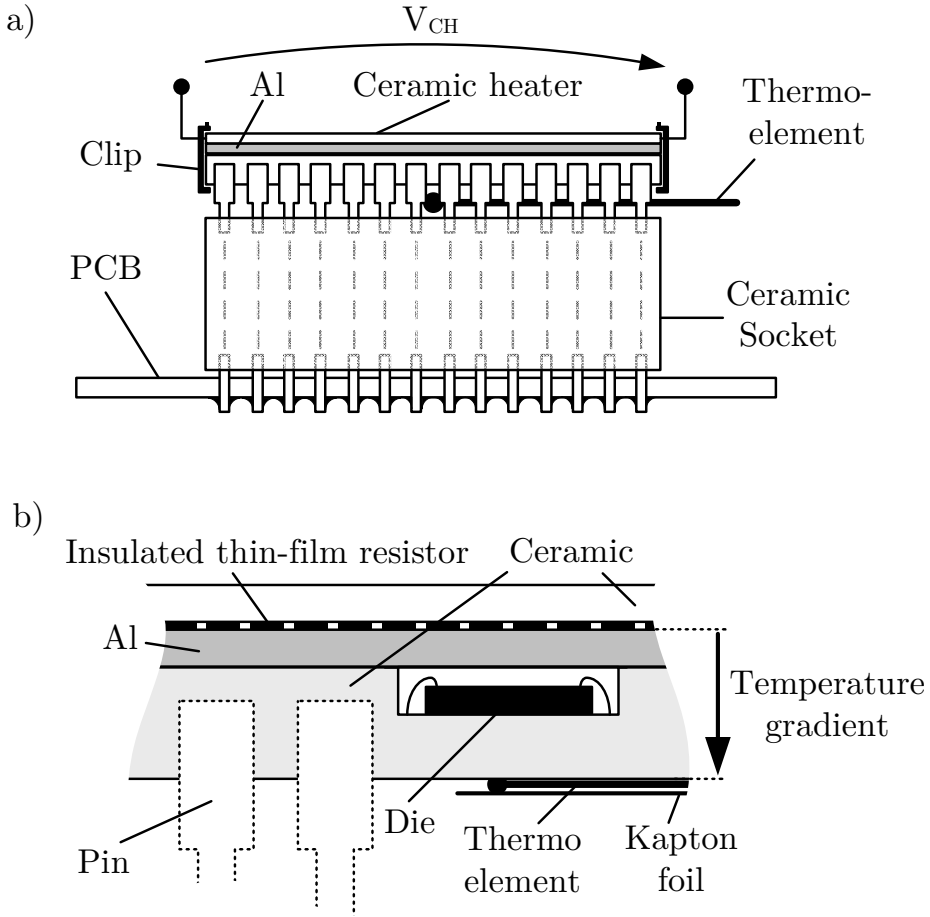

Figure A.2: a) Ceramic chip-package heater with ceramic socket and PCB. b) Closeup of die inside chip-package and temperature gradient.

A voltage source V_{CH} is used to power the ceramic heater. The heating element is realized as a thin film resistor deposited on a ceramic plate. The generated heat is spread across the chip by an aluminum plate. Figure A.2 b) shows a closeup of the setup. The temperature is measured with a thermo-element at the bottom side of the chip. The thermo-element is fixed to the chip using Kapton foil. Due to a temperature gradient from the heating resistor to the thermo-element, the expected die temperature is higher than the temperature measured at the bottom side of the chip. Measurements were started after a hold time of 5 min after a certain temperature was reached. It is expected that this time period is sufficient for the temperature to reach the silicon die within the package. Nevertheless, a temperature error of +2 % up to 400 °C has to be considered for these measurements.

Appendix B

Evaluation of Experimental Results

All experimental results of SOI-MOSFET device measurements were evaluated using MATLAB v7.0.4. After the data was exported from ICS to Excel, it was read and further processed using MATLAB.

B.1 SOI-MOSFET Characterization

The evaluation code of an N-channel SOI-MOSFET is given in listing B.1. The entire evaluation was realized in a single MATLAB file. The variable `Select` was used to choose between the different characterization procedures. The `gradient` function was used for the partial derivative, which was required e.g. for g_m or g_d. To reduce signal noise for g_d and V_A measurements at very high temperatures, the Savitzky-Golay filter function `sgolayfilt` was used. It was assured that the filter does not change the overall signal waveform, thus only reduces the noise level of the signal to remain compatible to non-filtered results. Results for P-channel SOI-MOSFETs were obtained analogously and are not shown here.

Listing B.1: N-Channel SOI-MOSFET Characterization in MATLAB

```
1  clear all;
2  % Device dimensions:
3  W=8;
4  L=4.8;
5
6  % Select:
7  % 1 = Input characteristics + gm
8  % 2 = Output characteristics + gd
9  % 3 = Intrinsic Gain gm/gd
10 % 4 = gm/ID
11 % 5 = Vth over VBS over T for VD01
```

```
% 6 = Leakage Current
% 7 = VA
% 8 = n
% 9 = I_on/I_off over T

Select=9;
%------------------------------
%Savitzky-Golay Filter Parameter
polynomial_order =1;
frame_size = 13;
%------------------------------

n_VB0 =zeros(281,12);
n_VB1 =zeros(281,12);

figure;
temp_count = 1;

for Temp=50:25:400
path = sprintf('NHGATE_L4u8_W8u0_NH3_92_%02dC.xls',Temp);

in_VD5 = abs(xlsread(path,10,'K2:S282'));
in_VD3 = abs(xlsread(path,11,'K2:S282'));
in_VD01 = abs(xlsread(path,12,'K2:S282'));

out_VB1 = abs(xlsread(path,8,'B2:BP201'));
out_VB0 = abs(xlsread(path,9,'B2:BP201'));

id_ein = abs([in_VD01, in_VD3, in_VD5]);
id_aus = abs([out_VB0, out_VB1]);

VG = xlsread(path,10,'J2:J282');
VG = VG(:,[1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1]);

VD = xlsread(path,8,'A2:A201');
VD = VD(:,[1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1
    1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1
     1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1
    1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1])
    ;

%============ Global gm ====================
%===========================================
gm=zeros(281,27);

```

```
count =1;
while count < 28
    gm(1:end,count) = gradient(id_ein(1:end,count),VG(1:end,count));
    count=count+1;
end

%============ Global gd ==================
%=========================================
gd=zeros(200,134);
va=zeros(200,134);

%-------- OPTIONAL FILTER ------------
%id_aus =sgolayfilt(id_aus,polynomial_order,frame_size);
%---------------------------------------

count=1;
while count < 135
    gd(1:end,count) = gradient(id_aus(1:end,count),VD(1:end,count));
    va(1:end,count) = 1./gradient(log(id_aus(1:end,count)),VD(1:end,count)
        );
    count=count+1;
end

%-------- OPTIONAL FILTER ------------
% gd =sgolayfilt(gd,polynomial_order,frame_size);
% va =sgolayfilt(va,polynomial_order,frame_size);
%---------------------------------------

if Select ==1
%====== Input Characteristics =============
%=========================================

 subplot(2, 2, 1), plot(VG,id_ein,'b-','LineWidth',2 ); hold on;

 xlabel('VG');
 ylabel('ID');
 set(gca,'XScale','linear','YScale','linear');
 set(gca,'XGrid','on','YGrid','on');

 subplot(1,2,1), semilogy(VG(1:end,1),in_VD01(1:end,1),'b-','LineWidth',2
      ); hold on;

 xlabel('VG');
 ylabel('log(ID)');
 set(gca,'XScale','linear','YScale','linear');
```

```
96  set(gca,'XGrid','on','YGrid','on');
97  xlim([-2 5]);
98  ylim([1e-13 1e-4]);
99
100 subplot(1,2,1), semilogy(VG(1:end,1),in_VD01(1:end,9),'b-','LineWidth',2
        ); hold on;
101
102 xlabel('VG');
103 ylabel('log(ID)');
104 set(gca,'XScale','linear','YScale','linear');
105 set(gca,'XGrid','on','YGrid','on');
106 xlim([-2 5]);
107 ylim([1e-13 1e-4]);
108
109 plot(VG(1:end,1:9),gm(1:end,1:9),'b','LineWidth',2 ); hold on;
110 plot(VG(1:end,1:9),gm(1:end,10:18),'r','LineWidth',2 ); hold on;
111 xlabel('VG');
112 ylabel('gm');
113 set(gca,'XScale','log','YScale','log');
114 set(gca,'XGrid','on','YGrid','on');
115
116 elseif Select ==2
117 %====== Output Characteristics ============
118 %==========================================
119 figure;
120 subplot(1, 2, 1), plot(VD,id_aus,'b-','LineWidth',2 ); hold on;
121
122 xlabel('VD');
123 ylabel('ID');
124 set(gca,'XScale','linear','YScale','linear');
125 set(gca,'XGrid','on','YGrid','on');
126
127 subplot(1, 2, 2), semilogy(VD,id_aus,'b-','LineWidth',2 ); hold on;
128
129 xlabel('VD');
130 ylabel('log(ID)');
131 set(gca,'XScale','linear','YScale','linear');
132 set(gca,'XGrid','on','YGrid','on');
133
134 figure;
135 plot(VD,gd,'b','LineWidth',2 ); hold on;
136
137 xlabel('VD');
138 ylabel('gd');
139 set(gca,'XScale','log','YScale','log');
```

```
140 set(gca,'XGrid','on','YGrid','on');
141 axis([0 5 0.1 200]);
142
143 elseif Select ==3
144 %========== Intrinsic Gain A ============
145 %========================================
146 gm_A =zeros(67,6);
147 gd_A =zeros(67,6);
148 A =zeros(67,6);
149 id_A =zeros(67,6);
150
151 %-----Umformen gm-----
152 zeile_gm =81;
153 spalte_VB0_gm =1;
154 spalte_VB1_gm =9;
155 gm_A_zeile =1;
156 gm_A_VB0 =1;
157 gm_A_VB1 =4;
158
159 while spalte_VB1_gm < 28
160
161     while zeile_gm < 280
162         gm_A(gm_A_zeile,gm_A_VB0) = gm(zeile_gm,spalte_VB0_gm);
163         gm_A(gm_A_zeile,gm_A_VB1) = gm(zeile_gm,spalte_VB1_gm);
164
165         zeile_gm = zeile_gm+3;
166         gm_A_zeile = gm_A_zeile+1;
167     end
168
169     gm_A_VB0 = gm_A_VB0+1;
170     gm_A_VB1 = gm_A_VB1+1;
171     spalte_VB0_gm = spalte_VB0_gm+9;
172     spalte_VB1_gm = spalte_VB1_gm+9;
173     zeile_gm = 81;
174     gm_A_zeile = 1;
175 end
176
177 %----- Sort gd----- (Column 1-3=VB0; 4-6=VB-1)
178 gd_A(1:67,1) = gd(5,1:67);
179 gd_A(1:67,2) = gd(121,1:67);
180 gd_A(1:67,3) = gd(200,1:67);
181
182 gd_A(1:67,4) = gd(5,68:134);
183 gd_A(1:67,5) = gd(121,68:134);
184 gd_A(1:67,6) = gd(200,68:134);
```

```
185
186 %---- Sort A=gm/gd----
187 A = gm_A./gd_A;
188
189 id_A(1:67,1) = id_aus(5,1:67);
190 id_A(1:67,2) = id_aus(121,1:67);
191 id_A(1:67,3) = id_aus(200,1:67);
192
193 id_A(1:67,4) = id_aus(5,68:134);
194 id_A(1:67,5) = id_aus(121,68:134);
195 id_A(1:67,6) = id_aus(200,68:134);
196
197 %VB0
198 %subplot(1, 2, 1), plot(id_A(1:64,1)./(W./L),A(1:64,1),'b','LineWidth',2
        ); hold on; %VD01
199 subplot(2, 1, 1), plot(id_A(1:64,2)./(W./L),A(1:64,2),'r','LineWidth',2 )
        ; hold on; %VD3
200 %subplot(1, 2, 1), plot(id_A(1:64,3)./(W./L),A(1:64,3),'k','LineWidth',2
        ); hold on; %VD5
201
202 xlabel('Id/(W/L)');
203 ylabel('A');
204 set(gca,'XScale','log','YScale','log');
205 set(gca,'XGrid','on','YGrid','on');
206 xlim([1e-9 5e-5]);
207 ylim([100 2e4]);
208
209 %-VB1
210 %subplot(1, 2, 2), plot(id_A(1:64,4)./(W./L),A(1:64,4),'b','LineWidth',2
        ); hold on; %VD01
211 subplot(2, 1, 2), plot(id_A(1:64,5)./(W./L),A(1:64,5),'r','LineWidth',2 )
        ; hold on; %VD3
212 %subplot(1, 2, 2), plot(id_A(1:64,6)./(W./L),A(1:64,6),'k','LineWidth',2
        ); hold on; %VD5
213
214 xlabel('Id/(W/L)');
215 ylabel('A');
216 set(gca,'XScale','log','YScale','log');
217 set(gca,'XGrid','on','YGrid','on');
218 xlim([1e-9 5e-5]);
219 ylim([100 2e4]);
220
221 %============== gm/Id ====================
222 %=========================================
223 elseif Select ==4
```

```
224
225 gm_id_VB0 =zeros(281,3);
226 gm_id_VB1 =zeros(281,3);
227
228 id_VB0 =[id_ein(1:end,1),id_ein(1:end,10),id_ein(1:end,19)];
229 id_VB1 =[id_ein(1:end,9),id_ein(1:end,18),id_ein(1:end,27)];
230
231 %-------- OPTIONAL FILTER ------------
232 %id_VB0 =sgolayfilt(id_VB0,polynomial_order,frame_size);
233 %id_VB1 =sgolayfilt(id_VB1,polynomial_order,frame_size);
234 %---------------------------------------
235
236 VG_gmid = VG(1:end,1:3);
237
238 count_gmid =1;
239 while count_gmid < 4
240 gm_id_VB0(1:end,count_gmid) =gradient(log(id_VB0(1:end,count_gmid)),
      VG_gmid(1:end,count_gmid));
241 gm_id_VB1(1:end,count_gmid) =gradient(log(id_VB1(1:end,count_gmid)),
      VG_gmid(1:end,count_gmid));
242 count_gmid=count_gmid+1;
243 end
244
245 %-------- OPTIONAL FILTER ------------
246 %gm_id_VB0 =sgolayfilt(gm_id_VB0,polynomial_order,frame_size);
247 %gm_id_VB1 =sgolayfilt(gm_id_VB1,polynomial_order,frame_size);
248 %---------------------------------------
249
250 %Column 1=VD01; 2=VD3; 3=VD5 in gm_id and id_VB
251 plot(id_VB0(1:end,1)./(W./L),gm_id_VB0(1:end,1),'b-','LineWidth',2 );
      hold on;
252
253 xlabel('ID/(W/L)');
254 ylabel('gm/ID');
255 set(gca,'XScale','log','YScale','log');
256 set(gca,'XGrid','on','YGrid','on');
257 xlim([1e-8 1e-04]);
258 ylim([1e0 10]);
259
260 plot(id_VB1(1:end,1)./(W./L),gm_id_VB1(1:end,1),'r-','LineWidth',2 );
      hold on;
261
262 xlabel('ID/(W/L)');
263 ylabel('gm/ID');
264 set(gca,'XScale','log','YScale','log');
```

```
265 set(gca,'XGrid','on','YGrid','on');
266 xlim([1e-8 1e-04]);
267 ylim([1e0 10]);
268
269 elseif Select ==5
270 %========== Threshold voltage =============
271 %==========================================
272
273 %SQRT(id(VD01)) for tangent method
274 id_Vth =abs(in_VD01);
275
276 %gm or VG at VD01 and VB 0 ---> -1
277 gm_Vth =gm(1:end,1:9);
278 VG_Vth =VG(1:end,1:9);
279
280 %Max gm and row number
281 [value_gm,pos] = max(gm_Vth,[],1);
282
283 %Values of VG or Wurzel(id) at max gm
284 value_VG1 =zeros(2,9);
285 value_id_Vth1 =zeros(2,9);
286 value_VG2 =zeros(2,9);
287 value_id_Vth2 =zeros(2,9);
288
289 %Tangent at root(Id) over VG @Max[VG(gm_max)]
290 %9 times for all 9 VB
291 count_fit =1;
292 FIT =zeros(281,9);
293
294 while count_fit < 10
295
296     pos =pos-1;
297     value_VG1 =VG_Vth(pos,count_fit);
298     value_id_Vth1 =id_Vth(pos,count_fit);
299
300     pos =pos+2; %n+1
301     value_VG2 =VG_Vth(pos,count_fit);
302     value_id_Vth2 =id_Vth(pos,count_fit);
303
304     %extract slope
305     fit = polyfit([value_VG1;value_VG2],[value_id_Vth1;value_id_Vth2], 1);
306     %calc tangent
307     FIT(1:end,count_fit) = fit(2)+fit(1)*VG_Vth(1:end,1);
308
309     %calc root of tangent
```

```
310     Vth_nhgate(temp_count,count_fit) = roots(fit) + 0.05;
311
312     count_fit =count_fit+1;
313 end
314
315 elseif Select ==6
316 %============ Leakage current =============
317 %=========================================
318
319 count =1;
320
321     for count=[1,9]
322         IL(temp_count,count) = in_VD01(81,count); %@VG=0V -> 81
323         IL3(temp_count,count) = in_VD3(81,count); %@VG=0V -> 81
324         IL5(temp_count,count) = in_VD5(81,count); %@VG=0V -> 81
325     end
326
327 elseif Select ==7
328 %============== VA ========================
329 %=========================================
330
331 count =1;
332 % 41 ^= 1V; 81 ^= 2V; 121 ^= 3V; 161 ^= 4V
333
334     for count=[1:67]
335         VA(count,temp_count) = va(161,count);
336         id_VA(count,temp_count) = id_aus(161,count);
337
338         VA_VB1(count,temp_count) = va(161,count+67);
339         id_VA_VB1(count,temp_count) = id_aus(161,count+67);
340
341         VA_3(count,temp_count) = va(161,count);
342         id_VA_3(count,temp_count) = id_aus(161,count);
343
344         VA_VB1_3(count,temp_count) = va(161,count+67);
345         id_VA_VB1_3(count,temp_count) = id_aus(161,count+67);
346     end
347
348 elseif Select ==8
349 %=================== n ====================
350 %=========================================
351
352 id_VB0 =[id_ein(1:end,1),id_ein(1:end,10),id_ein(1:end,19)];
353 id_VB1 =[id_ein(1:end,9),id_ein(1:end,18),id_ein(1:end,27)];
354
```

```
355 VG_n = VG(1:end,1);
356
357 n_VB0(1:end,temp_count) = 1./(gradient(log(id_VB0(1:end,2)),VG_n(1:end,1)
        ).*Vt);%1./(gradient(id_VB0(1:end,1),0.025).*log(10).*Vt);
358 n_VB1(1:end,temp_count) = 1./(gradient(log(id_VB1(1:end,2)),VG_n(1:end,1)
        ).*Vt);%1./(gradient(id_VB1(1:end,1),0.025).*log(10).*Vt);
359
360 %Colums 1=VD01; 2=VD3; 3=VD5 in gm_id and id_VB
361  plot(VG_n(1:end,1),n_VB0(1:end,temp_count),'b-','LineWidth',2 ); hold on
         ;
362
363  xlabel('ID/(W/L)');
364  ylabel('gm/ID');
365  set(gca,'XScale','linear','YScale','linear');
366  set(gca,'XGrid','on','YGrid','on');
367
368  plot(VG_n(1:end,1),n_VB1(1:end,temp_count),'r-','LineWidth',2 ); hold on
         ;
369
370  xlabel('ID/(W/L)');
371  ylabel('gm/ID');
372  set(gca,'XScale','linear','YScale','linear');
373  set(gca,'XGrid','on','YGrid','on');
374
375 elseif Select ==9
376 %================== Ion/Ioff =============
377 %=========================================
378
379 I_off_VD01_BG0(temp_count,1:9) = in_VD01(81,1:9);
380 I_off_VD3_BG0(temp_count,1:9) = in_VD3(81,1:9);
381 I_off_VD5_BG0(temp_count,1:9) = in_VD5(81,1:9);
382
383 I_on_VD01_BG0(temp_count,1:9) = in_VD01(281,1:9);
384 I_on_VD3_BG0(temp_count,1:9) = in_VD3(281,1:9);
385 I_on_VD5_BG0(temp_count,1:9) = in_VD5(281,1:9);
386
387 else
388
389 end
390 temp_count = temp_count +1;
391 end
392
393 %=========================================
394 %============== PLOTS ====================
395 %=========================================
```

```
396
397 if Select == 6
398 Temp=[50:50:400]; %match top temperature range
399
400 plot(Temp,IL./(W./L),'r-',Temp,IL3./(W./L),'b-',Temp,IL5./(W./L),'g-' );
        hold on
401
402 xlabel('Temperature [řC]');
403 ylabel('I_d/(W/L) @ V_G_S=0V [A]');
404 set(gca,'XScale','linear','YScale','log');
405 set(gca,'XGrid','on','YGrid','on');
406 end
407
408 if Select == 7
409 Temp=[400:100:400]; %match top temperature range
410
411 plot(id_VA(1:end,1)./(W./L),VA(1:end,1),'r-','LineWidth',2 ); hold on
412
413 xlabel('ID');
414 ylabel('VA');
415 set(gca,'XScale','log','YScale','log');
416 set(gca,'XGrid','on','YGrid','on');
417 xlim([1e-7 5e-5]);
418 ylim([10e0 100]);
419 end
420
421 if Select == 8
422 Temp=[50:25:400]; %match top temperature range
423
424 plot(Temp(1:end),n_VB0(109,1:temp_count-1),'r-',Temp(1:end),n_VB1(109,1:
        temp_count-1),'b','LineWidth',2 ); hold on
425
426 xlabel('ID/(W/L)');
427 ylabel('gm/ID');
428 set(gca,'XScale','linear','YScale','log');
429 set(gca,'XGrid','on','YGrid','on');
430 %xlim([1e-9 5e-06]);
431 ylim([1e0 1e1]);
432 end
433
434 if Select == 5
435 Temp=[50:50:400]; %match top temperature range
436 VB=[0:-0.125:-1];
437 [Xn,Yn] = meshgrid(VB,Temp);
438
```

```
439 surf(Yn,Xn,Vth_nhgate,'EdgeColor','red'); hold on;
440
441 axis([175 200 -1 0 0.1 1.2]);
442 colormap(autumn);
443 rotate3d on;
444
445 xlabel('Temperatur /řC')
446 ylabel('V_b')
447 zlabel('V_t_h /V')
448 set(gca,'XScale','linear','YScale','linear');
449 set(gca,'XGrid','on','YGrid','on');
450 end
451
452 %---------- I_on/I_off over T ------------------
453 if Select == 9
454
455 Temp=[50:25:400]; %match top temperature range
456
457 plot(Temp,I_on_VD01_BG0(1:end,1)./I_off_VD01_BG0(1:end,1),'r','LineWidth'
        ,2 ); hold on
458 %subplot(2,2,1), plot(Temp,I_on_VD3_BG0(1:end,1)./I_off_VD3_BG0(1:end,1)
        ,'r','LineWidth',2 ); hold on
459 %subplot(2,2,1), plot(Temp,I_on_VD5_BG0(1:end,1)./I_off_VD5_BG0(1:end,1)
        ,'k','LineWidth',2 ); hold on
460
461 legend('V_D=0V','V_D=3V','V_D=5V');
462 xlabel('T');
463 ylabel('I_D');
464 set(gca,'XScale','linear','YScale','log');
465 set(gca,'XGrid','on','YGrid','on');
466
467 plot(Temp,I_on_VD01_BG0(1:end,9)./I_off_VD01_BG0(1:end,9),'b','LineWidth'
        ,2 ); hold on
468 %subplot(2,2,2), plot(Temp,I_on_VD3_BG0(1:end,9)./I_off_VD3_BG0(1:end,9)
        ,'r','LineWidth',2 ); hold on
469 %subplot(2,2,2), plot(Temp,I_on_VD5_BG0(1:end,9)./I_off_VD5_BG0(1:end,9)
        ,'k','LineWidth',2 ); hold on
470
471 legend('V_D=0V','V_D=3V','V_D=5V');
472 xlabel('T');
473 ylabel('I_D');
474 set(gca,'XScale','linear','YScale','log');
475 set(gca,'XGrid','on','YGrid','on');
476
477 end
```